Reg. No. | | | | | | | | | | | | |

Question Paper Code : 14119

M.E. DEGREE EXAMINATION, JANUARY 2015.

First Semester

VLSI Design

VL 7101 — VLSI SIGNAL PROCESSING

(Common to M.E. Applied Electronics, M.E. Electronics and Communication Engineering, and M.E. Digital Signal Processing)

(Regulation 2013)

Time : Three hours Maximum : 100 marks

Answer ALL questions.

PART A — (10 × 2 = 20 marks)

1. State the functions of Decimator and Expander.
2. Highlight on the various DSP algorithms and their applications.
3. How is parallel processing for low power implemented?
4. List the properties of Retiming.
5. What are the different forms of pipeline interleaving? State their limitations.
6. How does a Transmission gate operate?
7. List the limitations of pipelining of Adaptive Filters.
8. What is the need for Algorithm- Architecture Transformation?
9. List the properties of CSD number representation.
10. How is path balancing achieved?

PART B — (5 × 16 = 80 marks)

11. (a) (i) Explain Vector Quantization. (8)

(ii) Explain the operation of Binary Multipliers. (8)

Or

(b) (i) Analyze and synthesize Filter banks for DWT and IDWT. (8)

(ii) List the DSP technology requirements. (8)

12. (a) (i) Enumerate the design steps for a parallel FIR system. (8)

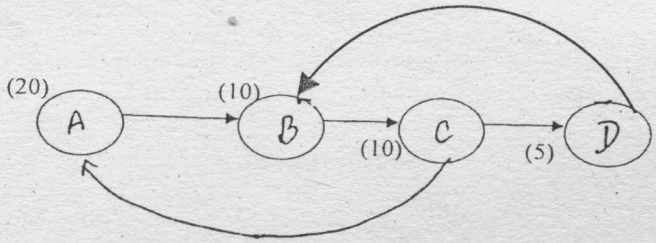
(ii) Consider the recursive filter $x(n)=\alpha x(n-2)+u(n)$.

Pipeline this multiply- add operator by 2 stages, by first breaking up the multiply-add operation into 2 components and by redistributing the delay elements in the loop. (8)

Or

(b) (i) With an example, explain Cutset retiming and pipelining. (8)

(ii) Consider the DFG shown in the figure below, where the number at each node denotes its execution time.



(1) What is the maximum sample rate of this DFG?

(2) What is the fundamental limit on the sample period for the system described by this DFG?

(3) Manually retime this DFG to minimize the clock period. (8)

13. (a) (i) In detail, explain COOK-TOOM algorithm. (8)

(ii) Construct a 3 x 3 fast convolution algorithm by inspection. (8)

Or

(b) (i) With the steps involved, explain the formulation of Parallel FIR Filtering using polyphase decomposition. (8)

(ii) Consider the IIR digital filter transfer function

$$H(z)=\frac{1}{1-\frac{4}{3}z^{-1}+\frac{5}{12}z^{-2}}$$

Obtain an equivalent 4 level pipelined transfer function using

(1) Clustered look ahead and

(2) Scattered look ahead. (8)

14. (a) (i) Explain the derivation of Basic Lattice filters using Reverse Schur polynomials. (8)

(ii) Obtain a 1-multiplier lattice structure for the second order transfer function

$$H(z)=\frac{\left(1+z^{-1}\right)^2}{1-3/\left(2\sqrt{2}\right)z^{-1}+9/16\,z^{-2}}.$$

The filter should be designed such that the numerator is expanded from the reverse Shur polynomial side. (8)

Or

(b) (i) Describe the steps for computation of round off noise for first order IIR filter. (8)

(ii) Compute the round off noise for the given second order IIR Filter with a scaling of M = 2

$$H(z)=\frac{1}{1-2r\cos\theta z^{-1}+r^2 z^{-2}}.$$ (8)

15. (a) (i) Explain with an example common subexpression elimination within a single multiplication. (8)

(ii) Explain the operation of synchronous pipelining and its clocking styles. (8)

Or

(b) (i) Discuss on constraint space diagram and degree of wave pipelining. (8)

(ii) Discuss on anyone type of power estimation approaches. (8)
