Reg. No. : | | | | | | | | | | | | |

Question Paper Code : 71874

M.E. DEGREE EXAMINATION, JUNE/JULY 2013.

Second Semester

Digital Signal Processing

VL 9253/10244 VLE 61/UVL 9151/VL 953 – VLSI SIGNAL PROCESSING

(Common to M.E. Applied Electronics and M.E. VLSI Design)

(Regulation 2009/2010)

Time : Three hours Maximum : 100 marks

Answer ALL questions.

PART A — ($10 \times 2 = 20$ marks)

1. Give some examples of common DSP algorithms and their applications.

2. Distinguish between signal flow graph and Dependence graph with example.

3. Mention the properties of unfolding.

4. What are Rank order filters?

5. List the steps involved in computing modified Cook-Toom algorithm.

6. Obtain 3-level pipelined transfer function for $H(z) = \frac{1}{1 - az^{-1}}$.

7. Define scaling and round- off noise.

8. Summarize the properties of Canonic Signed Digit representation.

9. What is sub–expression elimination process?

10. Define clock skew and propagation delay.

PART B — (5 × 16 = 80 marks)

11. (a) (i) Compute the iteration bound of the DFG given in figure 11 using LPM algorithm. (10)

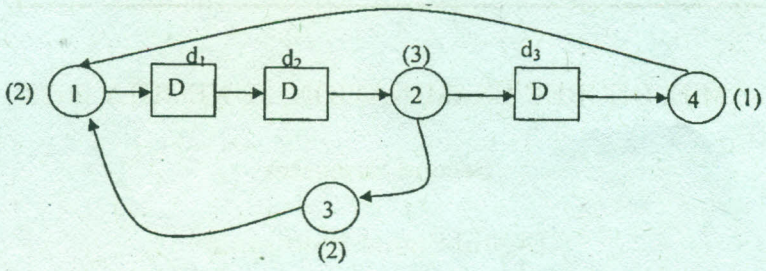

Figure 11

(ii) Explain the various representations of DSP algorithms with suitable diagrams. (6)

Or

(b) (i) Compute the iteration bound of the DFG given in. figure.11 using MCM algorithm. (10)

(ii) Discuss pipelining and parallel processing in designing low power systems. (6)

12. (a) Unfold the DFG given in figure 12 (a) using unfolding factor of 3 and 4. (16)

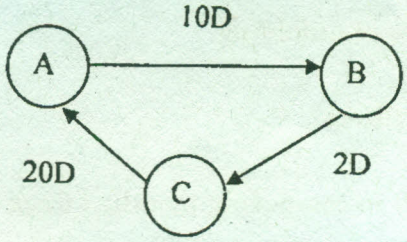

Figure 12 (a)

Or

(b) (i) Describe the method of formulation of two parallel fast FIR filtering using polyphase decomposition. (8)

(ii) Design a parallel rank order filter for window size w=7 and block size L=6.Calculate the number of C and S units. (8)

13. (a) Construct a 2x2 convolution algorithm using Cook Toom algorithm with β =0,1,2. (16)

Or

(b) Consider the 1st order IIR filter with transfer function $H(z)=\frac{1}{1-az^{-1}}$. Derive the filter structure with 4-level pipelining and 3-level block processing. (16)

14. (a) (i) Compute the state covariance for the unscaled 2nd order filter given in figure 14 a (i). (8)

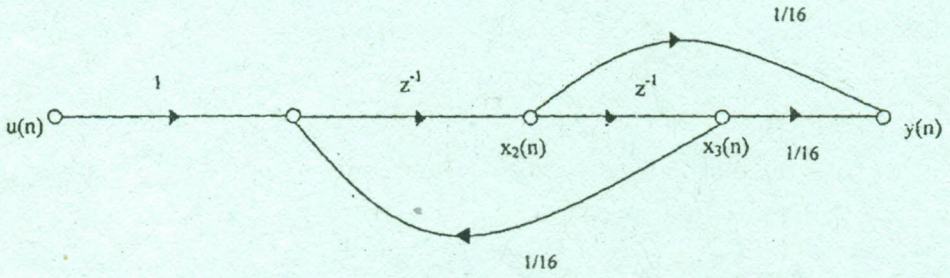

Figure 14 a (i)

(ii) Explain about the types of parallel multiplication with sign extension. (8)

Or

(b) (i) Briefly describe the design of lyon's bit serial multipliers using Horner's rule. (10)

(ii) Write short notes on Distributed Arithmetic operation. (6)

15. (a) (i) Demonstrate the process of reducing the hardware complexity using multiplicative splitting transformation on a transformation matrix

$$T=\begin{bmatrix} .4 & .7 & .4 \\ .6 & .8 & .2 \\ .1 & .3 & .2 \end{bmatrix}.$$ (8)

(ii) Explain row based and column based additive number splitting with example. (8)

Or

(b) (i) Explain wave pipelining and hence deduce an expression for the clock rate of the wave pipelined systems. (8)

(ii) Describe the concept of asynchronous pipelining and the protocol used between transmitter and receiver systems. (8)