Reg. No. :

Question Paper Code : 11918

M.E. DEGREE EXAMINATION, NOVEMBER/DECEMBER 2014.

Elective.

Applied Electronics

VL 9253/10244 VLE 61 — VLSI SIGNAL PROCESSING

(Common to M.E. VLSI Design)

(Regulation 2009/2010)

Time : Three hours

Maximum : 100 marks

Answer ALL questions.

PART A — $(10 \times 2 = 20 \text{ marks})$

1. Name two advantages of digital signal processing over analog.

2. What is iteration bound?

3. Prove that retiming does not change the number of delays in a cycle.

4. Draw the fine grain pipelined version of 3 tap FIR and calculate its critical path computation time.

5. Compare efficient single channel interleaving and multichannel interleaving in digital filters.

6. How does clustered look a head pipelining increase the sample rate by a factor M?

7. What are scaling and round off noise in a digital circuit?

8. State the properties of CST number representation.

9. What is iterative matching?

10. What are the effects of clock skew on synchronous sytems?

PART B — $(5 \times 16 = 80 \text{ marks})$

11. (a) Explain with suitable example the longest path matrix algorithm to compute iteration bound.

Or

- (b) Explain how pipelining and parallel processing help to realize low power circuits.
- 12. (a) (i) Describe an algorithm for unfolding.
 - (ii) Write a note on DCT architecture.

Or

- (b) (i) Discuss the implementation of 2-parallel FIR and two-parallel fast FIR filters with neat diagrams and expressions.
 - (ii) Write briefly about unfolding.
- 13. (a) Construct a 3×3 convolution algorithm using modified cook toom algorithm with ' β_i 's as 0, 1, -1, 2, -2. Mention the merits of pipelined and parallel recerisive filters.

Or

(b) Explain the register minimization in folded architecture for an IIR filter that computes.

y(n) = ay(n-3) + by(n-5) + x(n).

14. (a) Discuss round off noise in pipelined IIR filters.

Or

- (b) Discuss Lyon's but serial multiplier.
- 15. (a) With examples, show how subexpression elimination is applied to multipliers to reduce hardware.

Or

(b) Explain the wave-pipelined architecture and discuss on its limitation and advantages.