Reg. No. | | | | | | | | | | | | |

Question Paper Code : 14120

M.E. DEGREE EXAMINATION, JANUARY 2015.

Elective

VLSI Design

VL 7102 – VLSI DESIGN TECHNIQUES

(Common to M.E. Applied Electronics and M.E. Medical Electronics)

(Regulation 2013)

Time : Three hours Maximum : 100 marks

Answer ALL questions.

PART A — (10 × 2 = 20 marks)

1. Define Body effect.
2. State the various parameters which affect the threshold voltage of MOSFET.
3. Explain latch-up in CMOS circuits.
4. Draw the stick diagram of 2-input CMOS NAND gate.
5. Design a 2-input XOR using transmission gate.
6. What is the time delay associated with a CMOS inverter whose $\frac{(L/W)p.u}{(L/W)p.d} = 1.1$?
7. Define charge sharing.
8. State the various sources of power dissipation in CMOS.
9. What is the need for testing?
10. Explain the delay associated with a carry look ahead adder.

PART B — (5 × 16 = 80 marks)

11. (a) Derive an expression for the drain-to-source current, trans-conductance in linear and in the saturated region. Also derive an expression for the figure of merit and threshold voltage.

Or

(b) Explain in detail the small signal analysis of MOSFET by considering the effect of MOS gate capacitance and MOS diffusion capacitance.

12. (a) Explain the various methods which can be used to fabricate a CMOS. With neat diagram explain the steps involved in the fabrication of CMOS n-well process.

Or

(b) Define design rules. State the minimum width and minimum spacing rules of all MOS layers to draw the layout. Also draw the layout of CMOS inverter.

13. (a) Explain and draw the DC characteristics of CMOS inverter. Derive an expression for Ids in the five different regions of operation.

Or

(b) Design a 2-input CMOS NAND gate based on the following logic structures: Static CMOS logic, Transmission Gate, Pseudo-nMOS logic, Dynamic logic and using depletion load as the pull-up.

14. (a) (i) Estimate the pull-up and pull-down resistance of an nMOS inverter with $\frac{(L/W)p.u}{(L/W)p.d} = 4:1$. (8)

(ii) Derive an expression for the rise time, fall time and the average propagation delay of a CMOS inverter. (8)

Or

(b) Define scaling. Mention the types of scaling. Explain the various device parameters of MOSFET wrt full scaling, constant voltage scaling and general scaling.

15. (a) (i) Design a 2-input NOR using 2:1 Mux. (4)

(ii) Design a 4:1 Mux using 2:1 Mux. (6)

(iii) Design a 8:1 Mux using 4:1 Mux and 2:1 Mux. (6)

Or

(b) Compare the various types of adder structures.

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