23- FN

Reg. No. | | | | | | | | | | | | | |

Question Paper Code : 66321

M.E. DEGREE EXAMINATION, DECEMBER 2015/JANUARY 2016

First Semester

VLSI Design

VL7102 – VLSI Design Techniques

(Regulations : 2013)

Time : Three Hours **[Maximum : 100 Marks**

Answer ALL questions.

PART A – (10 × 2 = 20 Marks)

1. Explain channel length modulation.
2. Define subthreshold slope.
3. Explain lambda based design rules and list its advantages or disadvantages.
4. What is the need to check design rules ?
5. What are the disadvantages of resistive load-nMOSFET logic ?
6. When compared to a resistive load inverter, what are the advantages of an enhancement load inverter ?
7. Explain sheet resistance.
8. What are the important sources of power consumption in a CMOS circuit ?
9. Explain the process of physical design.
10. What is design for test ?

PART – B (5 × 13 = 65 Marks)

11. (a) Consider a p-channel MOSFET with following parameters. The device parameters are as follows :

Oxide thickness 15 nm, channel length 180 nm, channel width 360 nm, carrier mobility 25 $cm^2V^{-1}s^{-1}$, dielectric constant of oxide is 3.9 ε_0 ($\varepsilon_0 = 8.854 \times 10^{-14}$ F/cm), threshold voltage –0.4 V. The source and bulk of pMOSFET are connected to 1.8 V.

(i) When gate voltage is 0.2 V, drain voltage is 0.1 V, what is the region of operation of the MOSFET ? Estimate drain current, drain conductance and transconductance.

(ii) When gate voltage is 1.0 V, drain voltage is 1.5 V, what is the region of operation of the MOSFET ? Estimate drain current, drain conductance and transconductance.

OR

(b) (i) Explain body bias effect. What is positive body bias effect and negative body bias effect ? What is the effect of body bias on the MOSFET performance and circuit performance ? Is body bias desirable ? What is the best way to control body bias effect ? **(8)**

(ii) Threshold voltage of an n-channel MOSFET at zero substrate bias is 0.4 V. The substrate doping of MOSFET is $10^{15}cm^{-3}$, oxide thickness is 10 nm. If the substrate is connected to –2 V, what is the change in threshold voltage ? Given that dielectric constant of silicon is 11.8 ε_0 ($\varepsilon_0 = 8.854 \times 10^{-14}$ F/cm), intrinsic carrier concentration of silicon is 1.5×10^{15} cm^{-3}. **(5)**

12. (a) (i) Explain various rules associated with stick diagrams. **(8)**

(ii) Draw stick diagram of a two input NOR gate. **(5)**

OR

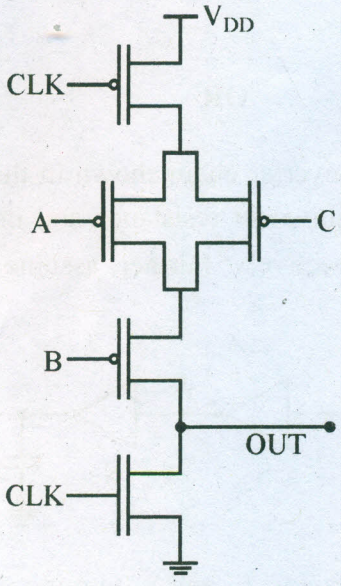
(b) Explain latch-up in CMOS circuits.

13. (a) Consider a resistive load nMOS inverter in 90 nm technology node has a load resistance of 30 kΩ. The oxide thickness is 3 nm. Electron mobility is $40cm^2V^{-1}s^{-1}$. Width, threshold voltage of nMOSFET are 450 nm and 0.4 V respectively. If the supply voltage is 1.3 V, find noise margins and switching threshold voltage of the inverter. Given that dielectric constant of oxide is 3.9 ε_0 ($\varepsilon_0 = 8.854 \times 10^{-14}$ F/cm).

OR

(b) Consider a static CMOS inverter in 90 nm technology node. The oxide thickness is 3 nm. Electron mobility 40 $cm^2V^{-1}s^{-1}$ is twice that of hole mobility. Width of pMOSFET and nMOSFET are 360 nm and 180 nm respectively. Threshold voltage of pMOSFET and nMOSFET are – 0.35 V and 0.4 V respectively. If the supply voltage is 1.3 V, find noise margins and switching threshold voltage of the inverter.

14. (a) Consider the logic circuit shown in the figure below.



(i) Write the Boolean function realized by the circuit and explain working of the circuit. **(4)**

(ii) What are the weaknesses of the circuit and explain the methods to overcome the weaknesses. **(9)**

OR

(b) Derive equation for raise time and fall time of a static CMOS inverter.

15. (a) Draw transistor level diagram of a NOR-based decoder circuit for two address bits and four word lines and explain its functionality.

OR

(b) Draw multiple-output domino CMOS representation of a Manchester carry chain.

PART – C (1 × 15 = 15 Marks)

16. (a) Consider function shown in eqn. (1)

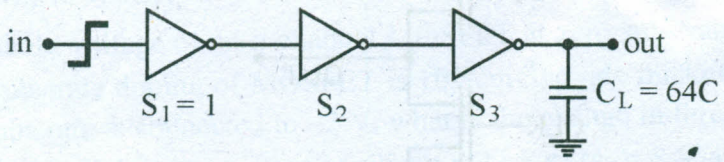
$$Y = \overline{A \bullet (B + C) + (D + E) \bullet (F + G)} \quad \text{(1)}$$

(i) Using static CMOS logic, implement function in eqn. (1). Assume that electron mobility is twice that of hole mobility.

(ii) Using domino-logic style logic, implement function in eqn. (1). Assume that electron mobility is twice that of hole mobility. What is the relative size of both circuits ?

OR

(b) Consider a static CMOS inverter chain shown in the figure below. Each inverter has symmetrical VTC. Equivalent resistance and input capacitance of unit-sized inverter are R and C, respectively. Further, assume that $C_{intrinsic} = C_{gate}$ ($\gamma = 1$). Sizing factor $S \geq 1$.



(i) Find the best sizing factors S_2 and S_3 to minimize propagation delay. **(2)**

(ii) What is the minimum delay (in terms of t_{p0}) ? **(1)**

(iii) What is the total energy drawn by second stage when the input changes from 0 to 1 (Symbolic answer in C, V) ? **(2)**

(iv) What is the energy dissipated as heat by the entire circuit (Symbolic answer in C, V) ? **(2)**