Reg. No. : | | | | | | | | | | | | |

Question Paper Code : 71869

M.E. DEGREE EXAMINATION, JUNE/JULY 2013.

First Semester

VLSI Design

VL 9212/VL 912/10244 VL 104 — VLSI DESIGN TECHNIQUES

(Common to M.E. Applied Electronics, M.E. VLSI Design and Embedded Systems, M.E. Digital Electronics and Communication Engineering and M.E. Digital Signal Processing)

(Regulation 2009/2010)

Time : Three hours Maximum : 100 marks

Answer ALL questions.

PART A — ($10 \times 2 = 20$ marks)

1. Draw the small signal model of MOS transistor.

2. Define body effect.

3. Draw the stick diagram of NOR gate using CMOS logic.

4. Determine the rise time of CMOS inverter. Let $\beta_p = 1.5$ mA/V^2, $V_{DD} = 3$V, $V_{tp} = 0.3$ V and load capacitance. $C_L = 1$ pF.

5. Determine the thin oxide capacitance, Cox per unit area. Let tox = 200 Å.

6. Define dynamic power dissipation of CMOS inverter.

7. Define observability of interconnect node in CMOS testing.

8. List out the goals of floor planning.

9. With suitable primitives develop the verilog module for a 2:1 multiplexer.

10. Write the data flow modeling of a 2 bit magnitude comparator.

PART B — (5 × 16 = 80 marks)

11. (a) (i) Design a 6-bit Dadda Multiplier. Compare its result with Wallace tree multiplier. (8)

(ii) Explain the Floor plan in detail. (8)

Or

(b) (i) Explain the power distribution of a chip. (8)

(ii) Design a 4-bit barrel shifter. (4)

(iii) Design a 8 × 1 Multiplexer. (4)

12. (a) (i) A precharge bus has a loading of 10 pF. At a point in the clock cycle, 64 registers with transmission gates on their inputs turn on. The input load of each register is 1 pF. Calculate the change in precharge voltage. (4)

(ii) Explain design margining in detail. (12)

Or

(b) (i) Explain the various types of power dissipation in detail. (12)

(ii) Explain delay time of CMOS inverter in detail. (4)

13. (a) (i) Explain DC transfer characteristics of CMOS inverter in detail. (12)

(ii) Discuss driving large capacitive load in detail. (4)

Or

(b) (i) Discuss super buffer in detail. (4)

(ii) Construct JK register using transmission gates. Explain its operation in detail. (8)

(iii) Explain dynamic CMOS design with an example. (4)

14. (a) (i) Discuss Change in threshold voltage due to body effect. (4)

(ii) Explain Id-Vds characteristics of NMOS inverter. (8)

(iii) Determine small signal parameters of MOS device. Let I_D = 0.8mA, V_A = 100 V, and β_n =1.5 mA/V^2. (4)

Or

(b) Explain CMOS process technology in detail. (16)

15. (a) (i) Write a Verilog code for the 4-bit adder/subtractor. (5)

(ii) Design a Verilog module for the master-slave flip flop. (5)

(iii) Write the test bench to verify the gate level modeling of SR latches. (6)

Or

(b) (i) Write the continuous assignment statements describing the following Boolean functions :

$$F(A,B,C)=\sum m(0,1,4,5,6,7).$$ (8)

(ii) Design a shift register by a synchronous cyclic behaviour with the list of procedural assignments. (8)