Reg. No. : | | | | | | | | | | | | |

Question Paper Code : 11913

M.E. DEGREE EXAMINATION, NOVEMBER/DECEMBER 2014.

First Semester

VLSI Design

VL 9212/VL 912/10244 VL 104 — VLSI DESIGN TECHNIQUES

(Common to M.E. Applied Electronics)

(Regulation 2009/2010)

Time : Three hours Maximum : 100 marks

Answer ALL questions.

PART A — (10 × 2 = 20 marks)

1. Distinguish between enhancement and depletion type MOSFET.

2. What are the physical parameters which affect the threshold voltage of a MSO structure?

3. Why is CMOS logic called as ratio less logic?

4. State the importance of power delay product,

5. Compare enhancement load inverter and depletion load inverter in terms of area.

6. How to estimate interconnect capacitance?

7. What are the advantages of carry look ahead adder?

8. Draw the circuit of a dynamic latch.

9. What are the advantages of hierarchical modelling?

10. What is the significance of test bench?

PART B — (5 × 16 = 80 marks)

11. (a) Derive the current equation for an channel MOS transistor operating in linear region. (16)

Or

(b) (i) Discuss about the MOS models and small signal AC characteristics. (12)

(ii) Explain the basics of CMOS technology. (4)

12. (a) With an aid of circuit diagram for a CMOS inverter explain the operation and sketch the voltage transfer characteristics and label all five critical voltages on the curve. (16)

Or

(b) Draw the circuit of an inverter with depletion type NMOS load and explain its operation with a voltage transfer curve. (16)

13. (a) Explain in detail how to estimate resistance and capacitance. (16)

Or

(b) (i) Explain in detail the supply voltage scaling in CMOS inverter. (8)

(ii) Discuss the three main components of power dissipation in CMOS inverter. (8)

14. (a) Design a 4 bit carry look ahead adder and explain its operation. (16)

Or

(b) Write explanatory notes on the following :

(i) Basics of CMOS testing. (8)

(ii) Delay modelling. (8)

15. (a) Write a Verilog program to design a 4 bit carry look ahead adder. (16)

Or

(b) Explain gate level and behavioural modelling. (16)

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