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Question Paper Code : 91848

M.E. DEGREE EXAMINATION, JANUARY 2012.

First Semester

Applied Electronics

VL 9212 — VLSI DESIGN TECHNIQUES

(Common to VLSI Design)

(Regulation 2009)

Time : Three hours Maximum : 100 marks

Answer ALL questions.

PART A — ($10 \times 2 = 20$ marks)

1. Explain why CMOS technology has become the dominant technology for VLSI.

2. How are n-well CMOS circuits superior to p-well CMOS circuits?

3. Draw the stick diagram of a 3-input AND gate.

4. What are the advantages of static CMOS circuits over dynamic CMOS circuits?

5. A particular layer of MOS circuit has a resistivity equal to 1 ohm cm. A section of this layer is 55 micro meter wide and has a thickness of 1 micro meter. Calculate the resistance from one end of this section to the other (along the length). Use the concept of sheet resistance R_s. What is the value of R_s?

6. What are the methods to reduce dynamic power?

7. Draw the circuit of 4×1 MUX using pass transistors.

8. What are stuck-at-faults?

9. Give the Verilog description of a 2 to 4 decoder.

10. Write a Verilog code to display a string on the screen.

PART B — ($5 \times 16 = 80$ marks)

11. (a) Explain the various second order effects seen in MOS transistors. (16)

Or

(b) List the various steps in the twin-tub fabrication process. Discuss its advantages. (16)

12. (a) Explain the transfer characteristics of a CMOS inverter. Derive an expression for its Noise margin. (16)

Or

(b) (i) Design the circuit of a full adder using transmission gates. (6)

(ii) Describe the structure of np-CMOS and Domino logic circuits with suitable examples. (10)

13. (a) Explain the switching characteristics of a CMOS inverter and derive expressions for rise-time and fall-time. (16)

Or

(b) (i) Explain the effects of scaling on device parameters. (8)

(ii) What is transistor sizing? How can it be used for power optimization? (8)

14. (a) (i) Describe the structure of carry look ahead adder and discuss its advantages and disadvantages. (8)

(ii) Explain the design of a 4-bit shift register. (8)

Or

(b) (i) Explain the goals and objectives of floor planning. (8)

(ii) Discuss the issues related to clock and power distribution. (8)

15. (a) What are the different modeling styles supported by Verilog HDL? Explain each style with an example. (16)

Or

(b) (i) Write the Verilog description of a sequence detector which can detect the sequence, 1010. (10)

(ii) Write a test bench program for a 2×1 MUX using Verilog HDL. (6)
