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Question Paper Code : 83355

M.E. DEGREE EXAMINATION, JANUARY 2014.

First Semester

VLSI Design

VL 7102 — VLSI DESIGN TECHNIQUES

(Regulation 2013)

Time : Three hours Maximum : 100 marks

Answer ALL questions.

PART A — (10 × 2 = 20 marks)

1. What is the modeling of MOS in the body effect?

2. Distinguish between junction leakage current and tunneling current.

3. Why do we use PMOS as a pull up device in a logic gate device?

4. Draw the CMOS structure for Tri state gate.

5. What do you observe in the transient analyzes of a inverter?

6. Draw the schematic diagram for transmission gate.

7. Write the modeling expression for the dynamic power dissipation.

8. Relate the power dissipation in a MOS due to thermal effect.

9. Write the unique feature of carry look ahead adder.

10. What do you mean by clock skew?

PART B — (5 × 16 = 80 marks)

11. (a) (i) Derive the modeling expression for a MOS diffusion capacitance. (10)

(ii) Discuss the temperature dependence of MOS transistor. (6)

Or

(b) List and discuss the non ideal effects which affect the ideal IV characteristics of MOS. (16)

12. (a) (i) Distinguish between latch and flipflop and explain how to synthesis in gate level. (10)

(ii) Sketch a complementary MOS gate circuit for computing three inputs NOR gate and show the stick diagram for the circuit. (6)

Or

(b) (i) Sketch a complementary MOS gate circuit for computing $Y = \overline{(A + B + C) \cdot D}$ and show the stick diagram for the circuit. (10)

(ii) Write the function of pass transistor. (6)

13. (a) Explain the modeling expression for considering a large load capacitor connected to an inverter. (16)

Or

(b) Explain the modeling expression for switching characteristics of an inverter for its L to H and H to L time. (16)

14. (a) Explain the static and dynamic power dissipation in MOS due to various factors. (16)

Or

(b) Explain the following in detail :

(i) Resistance estimation

(ii) Capacitance estimation

(iii) Transistor sizing and

(iv) Inductance estimation.

15. (a) Discuss the following circuit as VLSI system component level : (16)

(i) Multiplexer

(ii) Shift register

(iii) Encoder and

(iv) Decoder.

Or

(b) Discuss the power distribution subsystem in the MOS chip design. (16)

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