Reg. No. : ☐☐☐☐☐☐☐☐☐☐☐☐☐

Question Paper Code : 82132

M.E. DEGREE EXAMINATION, JUNE 2012.

Applied Electronics

VL 9212/10244 VL 104 — VLSI DESIGN TECHNIQUES

(Regulation 2009)

(Common to –M.E. VLSI Design)

Time : Three hours   Maximum : 100 marks

Answer ALL questions.

PART A — (10 × 2 = 20 marks)

1.   Give the advantage of CMOS technology.

2.   What is body effect in CMOS?

3.   Draw the stick diagram for an inverter.

4.   Define W/L Ratio.

5.   What is transistor sizing?

6.   What is charge sharing?

7.   Define physical design.

8.   What is floor planning?

9.   What is a test bench?

10. Write a verilog code to implement a half adder.

PART B — (5 × 16 = 80 marks)

11. (a) (i)   What is a threshold voltage? Derive its Equation and list the factors on which it is dependent. (8)

         (ii) Draw the saturated region and non saturated region of NMOS transistor and derive the expression for drain current. (8)

Or

     (b) Briefly explain the second order effects in CMOS. (16)

12. (a) (i)   What are the ways to reduce the power consumption of CMOS logic? (8)

         (ii) Derive the expression for Pull Up and Pull Down ratio for an NMOS inverter driven through one or more pass transistor. (8)

Or

     (b) Draw the stick diagram for Gray code to BCD converter. (16)

13. (a) Explain with a detailed note about the sizing of the transistor in relation with the switching Characteristics and fan-outs. (16)

Or

     (b) (i)   Enumerate the issues to be considered for circuit characterization and performance estimation. (8)

         (ii) Write short notes on capacitance estimation. (8)

14. (a) (i)   Briefly explain the implementation of carry look ahead adders. (8)

         (ii) Briefly explain the system level test techniques for VLSI system components. (8)

Or

     (b) (i)   Explain with diagram the design strategies for testing the CMOS devices. (8)

         (ii) Briefly explain the clock and power distribution in physical design. (8)

15. (a) (i)   Briefly explain the role of test bench in hardware description languages. (8)

         (ii) Write a verilog program to implement BCD to seven segment decoder. (8)

Or

     (b) (i)   Write a verilog program for implementing 4 bit ripple carry adder. (8)

         (ii) With an example program explain the difference between data flow and behavioral modelling. (8)