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**Question Paper Code : 71875**

M.E. DEGREE EXAMINATION, JUNE/JULY 2013.

Elective

VLSI Design

VL 9254/VL 954 — ANALOG VLSI DESIGN

(Common to M.E. Applied Electronics)

(Regulation 2009)

Time : Three hours

Maximum : 100 marks

Answer ALL questions.

PART A — (10 × 2 = 20 marks)

1. Write the applications of super MOS transistor.
2. Draw the primitive voltage follower and CMOS inverter cells.
3. Distinguish between flicker and thermal noises.
4. Draw a cascode current mirror.
5. Give the major differences between SC and SI filters.
6. Write the applications of interpolative modulators.
7. Write the need for fault modeling and simulation.
8. How do charge coupled devices differ from bucket-brigade-like devices?
9. State the major problems in producing mixed analog-digital layout.
10. Draw the CMOS transistor layout.

PART B — (5 × 16 = 80 marks)

11. (a) (i) Draw and explain the operation and design of a low voltage BiCMOS operational amplifier. (10)  
(ii) Draw and briefly explain a V-I converter. (6)

Or

- (b) (i) Explain the operation and implementation of a CMOS multiplier with necessary diagrams. (8)  
(ii) Give a brief note on low voltage filters. (8)
12. (a) (i) Explain the design of low power neural networks. (8)  
(ii) Discuss the design of switched current data converters and explain the practical considerations in SI circuits. (8)

Or

- (b) (i) Explain briefly the biologically inspired neural networks. (12)  
(ii) Give a brief note on contrast sensitive silicon retina. (4)
13. (a) (i) Describe the principle of bilinear transformation with necessary equations and diagrams and discuss its application in filter design. (8)  
(ii) Give a brief note on switched current filters. (8)

Or

- (b) (i) Discuss the first order and multi-bit sigma delta modulators. (10)  
(ii) Draw and briefly explain thermal and magnetic sensors. (6)
14. (a) (i) Compare ad hoc, boundary scan and built-in self test approaches. (10)  
(ii) Discuss the scaling of interconnects. (6)

Or

- (b) (i) Describe the resistance, capacitance and propagation delay of VLSI interconnects with suitable equations. (8)  
(ii) Explain a configurable architecture for prototyping analog circuit. (8)

15. (a) Write short notes on :

(i) Statistical device modeling (8)

(ii) Automating analog layout. (8)

Or

(b) (i) Describe about automating analog circuit design. (12)

(ii) Give a short account on capacitor layout. (4)

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