Reg. No. :

Question Paper Code : 71026

M.E. DEGREE EXAMINATION, JUNE/JULY 2013.

Second Semester

Applied Electronics

AP 9221/AP 921/10244 AE 201 — ANALYSIS AND DESIGN OF ANALOG INTEGRATED CIRCUITS

(Common to M.E. VLSI Design and Embedded Systems)

(Regulation 2009/2010)

Time : Three hours

Maximum: 100 marks

Answer ALL questions.

PART A — $(10 \times 2 = 20 \text{ marks})$

- 1. Draw the small signal model of the MOS transistor.
- 2. What are the short circuit effects in MOS transistor?
- 3. Compare & Contrast Emitter follower and source follower.
- 4. What is the need for an active load?
- 5. Define Slew rate.
- 6. What are the methods to achieve low input bias current in Op-Amps?
- 7. Define Noise figure.
- 8. What are the various sources of noise?
- 9. What is the reason for not using Beta-Helpers in simple MOS current mirrors to reduce the gain error?
- 10. Compare & Contrast MOS Op-Amps & Op-Amps using transistors.

PART B — $(5 \times 16 = 80 \text{ marks})$

11. (a) With an aid of small signal equivalent circuit of the bipolar transistor, derive the various elements in the small signal model.

Or

- (b) Explain depiction region of a PN Junction and derive for the total voltage across the junction.
- 12. (a) Explain the operation of a bipolar Widlar current source and find the output current and using small signal model derive its output resistance.

Or

- (b) Explain the working of a band gap reference bias circuit with necessary diagrams.
- 13. (a) What are the factors which limit slew rate in Op-Amp and explain the methods to improve slew rate.

Or

- (b) Determine the input resistance, output resistance and trans-conductance of 741 Op-Amp with an aid of small signal model.
- 14. (a) Derive the expression for the differential output current in Gilbert Multiplier which is suitable for four quadrant multiplication.

Or

- (b) Explain the principles and applications of PLL with necessary diagrams.
- 15. (a) Explain the two stage MOS operational amplifier with a neat sketch.

Or

(b) Write Explanatory note on (i) CMOS Class AB output Stage (ii) MOS Folded cascode op-amp. (8+8)