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**Question Paper Code : 11032**

M.E. DEGREE EXAMINATION, NOVEMBER/DECEMBER 2014.

Second Semester

Applied Electronics

AP 9221/ AP 921/ 10244 AE 201 — ANALYSIS AND DESIGN OF ANALOG INTEGRATED CIRCUITS

(Common to M.E. VLSI Design/ M.E. Electronics and Communication Engineering)

(Regulation 2009/2010)

Time : Three hours Maximum : 100 marks

Answer ALL questions.

PART A — (10 × 2 = 20 marks)

1. Compare $f_T$ of BJT and MOS devices.

2. What is weak inversion?

3. Design a simple CMOS current mirror and obtain its output impedance.

4. Design a band-gap referenced bias circuits using CMOS technology.

5. Define Slew rate

6. What are the methods to achieve low input bias current in Op-Amps?

7. Under what condition is a Gilbert multiplier used as balanced Modulator.

8. Define noise figure.

9. Why is source degeneration rarely used in MOS current mirrors?

10. How does a source follower act as a output stage?

PART B — (5 × 16 = 80 marks)

11. (a) Derive the expression for the small signal circuit elements of Bipolar transistor with an aid of small signal model.

Or

(b) Explain about the short channel effects in MOS transistors.

12. (a) Design a self biased $V_{BE}$ reference circuit with necessary diagrams and test the supply independence and temperature independence of the output current.

Or

(b) Derive the expression for CMRR of an emitter coupled differential amplifier with active load.

13. (a) Explain the operation of a two stage op-amp and derive for its over all gain and unity gain frequency.

Or

(b) (i) Using Miller approximation, calculate the 3-dB frequency of a common-source transistor stage using the following specifications. $R_S = 11_{cr}$, $I_D = 1mA$, $K'W/L = 100\,mA/V^2$ $f_T = 400MHz$ at $I_D = 1mA$ $C_{gd} = 0.5pF$ $C_{gb} = 0$ $R_L = 5\Omega$. (8)

(ii) Plot the frequency response of common mode gain, differential mode gain and CMRR for differential amplifier. Explain its variations with the frequency of the gain parameters. (8)

14. (a) Explain the Gilbert multiplier cell and discuss its operation as four quadrant multiplier.

Or

(b) (i) Explain the role of VCO in PLL. (8)

(ii) What are the various types of noises present in integrated circuits? Draw the MOS-FET small signal equivalent circuit with noise sources and explain. (8)

15. (a) Explain the two stage MOS operational amplifier with a neat sketch.

Or

(b) Write Explanatory note on (i) CMOS Class AB output Stage (ii) MOS Folded cascode op-amp. (8+8)

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