Reg. No. | | | | | | | | | | | | |

Question Paper Code : 86074

M.E. DEGREE EXAMINATION, MAY/JUNE 2016

Second Semester

Applied Electronics

AP 7201 – ANALYSIS AND DESIGN OF ANALOG INTEGRATED CIRCUITS

(Common to M.E. VLSI Design)

(Regulations 2013)

Time : Three Hours **Maximum : 100 Marks**

Answer ALL questions.

PART – A (10 × 2 = 20 Marks)

1. Define the common gate stage with direct coupling and capacitive coupling at input.

2. Sketch the small signal differential gain of a differential pair as a function of the input CM level.

3. List the statistical characteristics of noise.

4. What factors affect the frequency response of Common Source stage?

5. Define Slew rate and state its significance.

6. List the advantages of negative feedback?

7. State the importance of phase margin in Op Amp design.

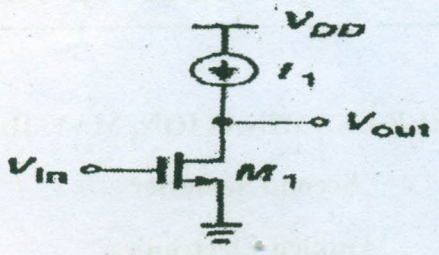
8. Mention any one method for improving slew rate.

9. What is the effect of channel length modulation on the current mirror ratio?

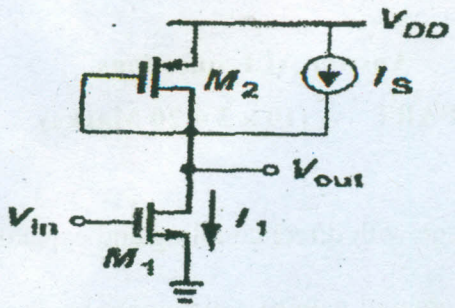
10. State principle of PTAT current generation.

PART – B (5 × 13 = 65 Marks)

11. (a) (i) Assuming M_1, in the following figure is biased in saturation, calculate the small signal voltage gain of the circuit. (7)

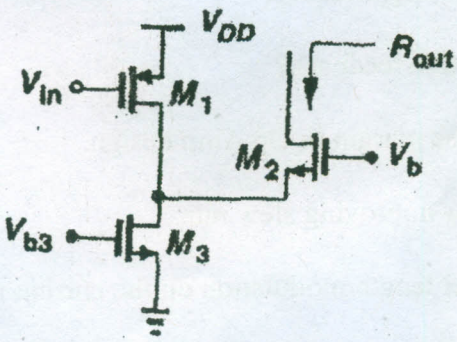


(ii) In the circuit shown below, M_1 is biased in saturation with a drain current equal to I_s. The current source $I_s = 0.75\ I_1$ is added to the circuit. How is it modified for this case ? (6)

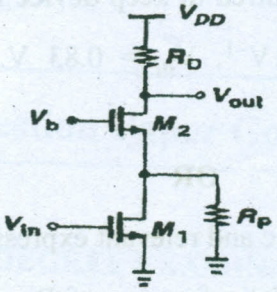


OR

(b) (i) Calculate the output impedance of the folded cascade shown in following figure where M_3 operates as a current source. (7)



(ii) Calculate the Voltage gain of the circuit shown below. (6)



12. (a) Design a two stage operational amplifier considering the open loop transfer function with higher order poles and zeros. Determine its phase margin, Q factor with dominant pole wp1, higher order pole wp2, zero w2.

OR

(b) Discuss the effect of noise in Differential amplifier and explain the techniques available to reduce the same.

13. (a) Explain the effect of loading in current- voltage feedback network using z^* Model.

OR

(b) Compare telescopic and folded cascade topologies of single stage op amp and discuss the effect of gain boosting in cascade devices.

14. (a) Construct the root locus for a two pole system.

OR

(b) Explain compensation methods of two stage op amps in detail.

15. (a) (i) Design DC current sources with current values of 10μA and 20μA and DC current sinks with current values of 10 μA and 40 μA. V_{DS} sat for both currents sinks and sources must be less than 0.5V. You are given one reference current source of 10 μA. $V_{TN} = 1V$, $V_{TP} = -1V$, $\mu_N C_{ox} = 50$ $\mu A/V^2$, $\mu_p C_{ox} = 25\ \mu A/V^2$, $\lambda_n = \lambda_p = 0.1V^{-1}$ at L = 1 μm.

(ii) For the source generated current mirror calculate output resistance and minimum voltage required to keep device in saturation $\mu_n C_{ox}$ W/L = 110 $\mu A/V^2$ and $\lambda = 0.01V^{-1}$, V_{th} = 0.83 V. Also draw the small signal equivalent circuit.

OR

(b) (i) Explain with schematic and relevant expressions of constant gm biasing.

(ii) Discuss the characteristic features of BandGap Reference circuit. Show how it yields temperature independent biasing.

PART – B (1 × 15 = 15 Marks)

16. (a) Enumerate the various factors that limit the slew rate of op amps and critically examine any two methods for improving the same. **(15)**

OR

(b) (i) Calculate input common mode voltage range and closed loop output impedance for Cascode Opamp. **(8)**

(ii) Explain and critically examine the effect of loading in feedback networks. **(7)**

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