Reg. No. | | | | | | | | | | | | |

Question Paper Code : 87272

M.E. DEGREE EXAMINATION, MAY/JUNE 2016

Second Semester

VLSI Design

VL 7201 – CAD FOR VLSI CIRCUITS

(Common to M.E. Applied Electronics)

(Regulations 2013)

Time : Three Hours **Maximum : 100 Marks**

Answer ALL questions.

PART – A (10 × 2 = 20 Marks)

1. Sketch and visualize the three design domains in Gajski's Y-chart.

2. For the graph shown in Fig. 1, apply Prim's algorithm and obtain the minimum spanning tree.

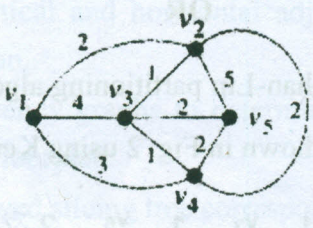

Fig. – 1

3. Draw the symbolic layout of 2 input CMOS NAND gate.

4. Write the template for circuit representation using data structure definitions.

5. List out the most important parameters used to characterise the local routing problems.

6. Highlight the significance of shape functions in floor planning.

7. Write the data structures to be used for the description of a switch-level simulation algorithm.

8. Sketch the two possible ROBDDs for the given function $f = (x_1 \oplus x_2) \cdot (x_3 \oplus x_4)$.

9. Draw the most serial DFG representation for the given function $f = a + b + c + d$.

10. What are the various hardware components used in a high-level synthesis system ?

PART – B (5 × 13 = 65 Marks)

11. (a) Briefly mention the most relevant tools used in VLSI design automation.

OR

(b) Indicate how genetic alogirthms can be used to optimize solutions related to search problems.

12. (a) With suitable example, explain the iterative placement algorithm.

OR

(b) Discuss about the Kernighan-Lin partitioning algorithm along with pseudo code. Also partition the graph shown in Fig. 2 using Kernighan-Lin algorithm.

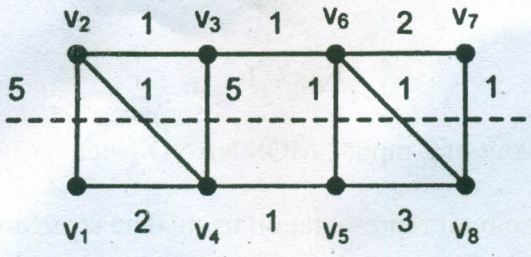

Fig. – 2

13. (a) For the rectangular floorplan of Fig. 3 assume the cells have the sizes as given in table 1.

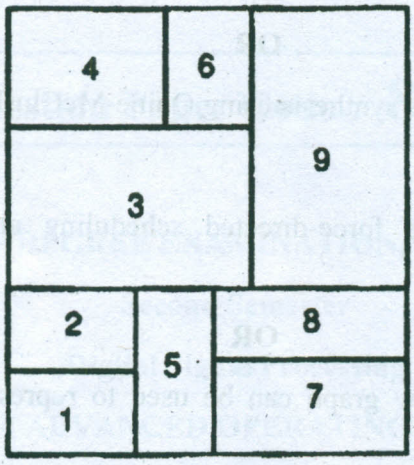

Fig. – 3

Module No.	Width	Height
1	2	1
2	2	2
3	4	3
4	3	1
5	1	3
6	1	1
7	3	2
8	3	1
9	2	4

(i) Draw the vertical and horizontal adjacency graphs corresponding to the above floorplan.

(ii) Use the adjacency graphs to determine the minimum required width and height of the floorplan.

(iii) Draw the skewed slicing tree corresponding to the above slicing floorplan.

(iv) Determine the normalized polish expression corresponding to the skewed slicing tree of (iii).

(v) Assume that all cells are rigid and have fixed orientations. Use the slicing tree of (iii) and the given cells sizes to find the area and dimensions of the smallest bounding rectangle of the given slicing floorplan.

OR

(b) Explain Rectilinear Steiner-tree algorithm with necessary pseudo codes.

14. (a) Describe event driven simulation method with suitable implementation mechanism.

OR

(b) Explain two-level logic synthesis using Quine-McCluskey algorithm.

15. (a) Discuss in detail the force-directed scheduling algorithm with a suitable example.

OR

(b) Explain how data flow graph can be used to represent an algorithm with an example.

PART-C (1 × 15 = 15 Marks)

16. (a) Explain in detail the depth-first search and breadth-first search algorithms using relevant pseudo codes. Also obtain the traversal paths of both algorithms in the directed graph shown in Fig. 4.

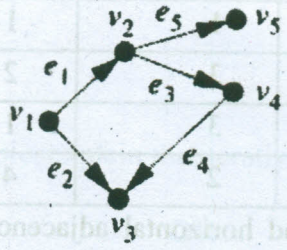

Fig. – 4

OR

(b) Given the following instance of the channel routing problem :

Top = [2, 1, 5, 1, 2, 3, 6]

Bot = [5, 3, 6, 4, 0, 2, 4]

(i) Determine the maximal sets and find a lower bound on the channel width.

(ii) Draw the horizontal constraint graph and vertical constraint graph.

(iii) Apply the constrain left edge algorithm to route the channel.