ANNA UNIVERSITY COIMBATORE

M.E / M.TECH. DEGREE EXAMINATIONS : **JUNE – JULY 2009**

REGULATIONS - 2007

SECOND SEMESTER

071280040 / 071290038 – COMPUTER AIDED DESIGN OF VLSI CIRCUITS

(COMMON TO APPLIED ELECTRONICS / VLSI DESIGN)

TIME : 3 HOURS **MAX.MARKS : 100**

PART A

(20 x 2 = 40 MARKS)

ANSWER ALL QUESTIONS

1. Draw the design flow of the VLSI chip technology.
2. How will you classify the VLSI design automation tools?
3. List the different optimization techniques used in VLSI.
4. Define tractable and untractable problems.
5. What is the need for layout compaction?
6. What is the use of λ cut rule?
7. What do you mean by prelayout simulation in VLSI?
8. Draw the node graph of D-latch.
9. How will you choose the shape for implementing a circuit in a chip?
10. Find out chip size to implement the following cells :

    A : 3 x 5

    B : 4 x 6
11. What is area routing?
12. Name the algorithms for global routing.
13. Define synthesis of a VLSI circuits.

14. What is delta delay? Mention its significance.
15. What is BDD? What are the advantages of BDD?
16. Name the tools used for gate level and switch level modeling.
17. What do you mean by high level synthesis?
18. What is scheduling? List the advantages of scheduling.
19. What is 'Clique Partitioning'? Where it is used?
20. What is 'retiming transformation'? Illustrate with example.

PART – B

(5 x 12 = 60 MARKS)

ANSWER ANY FIVE QUESTIONS

21. Explain in detail about the different optimization techniques used in VLSI circuits. (12)

22.a) Explain Kernighan – Lin partitioning algorithm with pseudocode description. (6)

b)Explain the different placement algorithm in detail. (6)

23.a) Explain in detail about area routing. (6)

b) Discuss the use of shape functions in floor planning. (6)

24.a) What is global routing? Discuss the use of rectilinear tree in global routing. (8)

b) What is global routing in standard cell layout? (4)

25. Explain in detail about the gate level modeling and simulation. (12)

26.a) Discuss the two level logic synthesis in detail. (8)

b) Explain the advantages of ROBDD with an example. (4)

27.a) How a data flow graph is represented? Apply the data flow graph for a second order digital filter. (8)

b) Draw and lable the various hardware component that can be used by a high level synthesis system. (4)

28. Discuss the different scheduling algorithm with an example. (12)

*****THE END*****