Reg. No. : | | | | | | | | | | | | |

Question Paper Code : 81034

M.E. DEGREE EXAMINATION, JUNE 2012.

Second Semester

Applied Electronics/ AP 9222/248205/AP 922/10244 AE 202 — COMPUTER ARCHITECTURE AND PARALLEL PROCESSING

(Common to M.E. Computer and Communication, M.E. VLSI Design and M.E. Embedded System Technologies)

(Regulation 2009)

Time : Three hours Maximum : 100 marks

Answer ALL questions.

PART A — ($10 \times 2 = 20$ marks)

1. What are the metrics used for measuring the performance of parallel systems?

2. What is the difference between a binary K-cube and a cube connected network of degree K?

3. Is it possible for the average speedup exhibited by a parallel algorithm to be super linear?

4. Given a task graph and arbitrarily large number of processors, what is a lower bound on the length of an optimal schedule?

5. Name the various memory update policies.

6. What is the need for memory hierarchy?

7. What are the two types of data flow architectures?

8. Compare multi vector and SIMD computers.

9. Name any two SIMD languages.

10. Differentiate between SIMD and SPMD programming.

PART B — (5 × 16 = 80 marks)

11. (a) (i) Explain the PRAM and VLSI model of parallel computation. (8)

(ii) List the conditions of parallelism. (8)

Or

(b) Discuss the various computer architectural classification schemes with suitable diagrams. (16)

12. (a) (i) Consider a PXM cross bar switch connecting P procesors to m memory modules. Assume only one input AND gate and OR gate. Assume that all variables are available in true and complement forms. Estimate the number of gates in the switch. Assume the data width to be W bits. (8)

(ii) List the parallel processing applications in various domains. (8)

Or

(b) Discuss the merits and demerits of various partitioning and scheduling techniques for parallel environment. (16)

13. (a) In a uniprocessor with cache, the processor issues its memory access requests to cache controller (CC). In case of miss or write through, CC interacts with memory controller (MC). Draw the flow charts describing the operation of CC for a read and a write operation for:

(i) WBWA

(ii) WTWA

(iii) Write through without write allocation. (16)

Or

(b) Explain paged memory and memory with paged segments virtual memory system. (16)

14. (a) (i) Draw and explain the types of multiprocessor and multicomputer architectures. (10)

(ii) Draw the architecture of de Brigin networks and shuffle exchange networks. (6)

Or

(b) Discuss the merits and demerits of types of scalar, multithreaded and data flow architectures. (16)

15. (a) Write the matrix multiplication algorithm for 2-D mesh and hypercube SIMD models. (16)

Or

(b) Write about the parallel constructs provided by any four languages with example. (16)
