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Question Paper Code : 71027

M.E. DEGREE EXAMINATION, JUNE/JULY 2013.

Second Semester

Applied Electronics

AP 9222/AP 922/UAP 9154/10244 AE 202 – COMPUTER ARCHITECTURE AND PARALLEL PROCESSING

(Common to M.E. Computer and Communication, M.E. VLSI Design, M.E. Embedded System Technologies and M.E. Digital Electronics and Communication Engineering)

(Regulation 2009/2010)

Time : Three hours Maximum : 100 marks

Answer ALL questions.

PART A — ($10 \times 2 = 20$ marks)

1. Give the technology and architecture of third generation computers.

2. List the three shared memory multiprocessor models.

3. Define computational granularity and I/O dependence with reference to parallelism and dependence relations

4. What do understand by cross bar networks?

5. Compare and contrast a processor and a coprocessor.

6. What do you understand by
   (a) Arbitration
   (b) Interrupt.

7. What is a linear pipeline processor?

8. List the branch prediction techniques in pipelined processors.

9. Distinguish between synchronous and asynchronous message passing schemes of multi computers.

10. Define multiprocessing. Mention the two types.

PART B — (5 × 16 = 80 marks)

11. (a) (i) Draw the tree showing architectural evolution from sequential scalar computers to vector processors and parallel computers and comment on the same. (8)

(ii) With a sketch of the architecture of a vector super computer. Explain how it is an operational feature for a scalar processor. (8)

Or

(b) Explain how instruction set, compiler technology, CPU implementation and control, and cache and memory hierarchy affect the CPU performance And justify the effects in terms of program length, clock rate and effective CPI. (16)

12. (a) Answer the following questions on program flow mechanisms and computer models:

(i) Compare control-flow data flow, and reduction computers in terms of the program flow mechanism used. (6)

(ii) Comment on the advantages and disadvantages in control complexity, potential for parallelism, and cost-effectiveness of the above computer models. (6)

(iii) What are the differences between string reduction and graph reduction machines? (4)

Or

(b) Discuss and analyze the scalability of parallel algorithms with respect to key machine classes. (16)

13. (a) Answer the following questions on designing scalar RISC or superscalar RISC processors :

(i) Why do most RISC integer units use 32 general-purpose registers? Explain the concept of register windows implemented in the SPARC architecture. (6)

(ii) What are the design tradeoffs between a large register file and a large D-cache? Why are reservation stations or reorder buffers needed in a superscalar processor? (6)

(iii) Explain the relationship between the integer unit and the floating-point unit in most RISC processors with scalar or superscalar organization. (4)

Or

(b) (i) Compare the relative merits of the four cache memory organizations : (4)

Direct-mapping cache.

Fully associative cache

Set-associative cache

Sector mapping cache.

(ii) Consider a main memory consisting of four memory modules with 256 words per module. Assume 16 words in each cache block. The cache has a total capacity of 256 words. Set-associative mapping is used to allocate cache blocks to block frames. The cache is divided into four sets.

(1) Show the address assignment for all 1024 works in a four-way low-order interleaved organization of the main memory. (3)

(2) How many blocks are there in the main memory? How many block frames are there in the cache? (3)

(3) Explain the bit fields needed for addressing each word in the two-level memory system. (3)

(4) Show the mapping from the blocks in the main memory to the sets in the cache and explain how to use the tag field to locate a block frame within each set. (3)

14. (a) (i) Discuss the two categories of linear pipeline based on the control of data flow along the pipeline. (8)

(ii) Consider the execution of a program of 15,000 instructions by a linear pipeline processor with a clock rate of 25MHz. Assume that the instruction pipeline has five stages and that one instruction is issued per clock cycle. The penalties due to branch instructions and out-of-sequence executions are ignored.

(1) Calculate the speedup factor in using this pipeline to execute the program as compared with the use of an equivalent non-pipelined processor with an equal amount of flow-through delay. (4)

(2) What are the efficiency and throughput of this pipelined processor? (4)

Or

(b) (i) Considering the Arithmetic principles, explain how pipeline techniques can be applied to speed up arithmetic computations both fixed point and floating point operation. (10)

(ii) Compare a carry propagate adder and a carry save adder with appropriate diagrams. (6)

15. (a) Elaborate on the five programming model that exploit parallelism with different execution paradigms. (16)

Or

(b) Write short notes on

(i) Language features for parallelism (8)

(ii) Optimizing compilers for parallelism. (8)
