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Question Paper Code : 82136

M.E. DEGREE EXAMINATION, JUNE 2012.

Elective

VLSI Design

VL 9252 / 252072 / VL 952 / 10244 VLE 51 — LOW POWER VLSI DESIGN

(Common to M.E. Applied Electronics)

(Regulation 2009)

Time : Three hours Maximum : 100 marks

Answer ALL questions.

PART A — (10 × 2 = 20 marks)

1. How does length of channel affect power dissipation in CMOS circuit?

2. Name the three sources of power dissipation in CMOS digital circuits.

3. What are the four components associated with circuit level optimization algorithms?

4. What is transistor sizing?

5. Why is pseudo-nmos called ratioed logic?

6. Compare DCSL and DCVS logic.

7. Define static probability and transition density.

8. Draw the model which depicts the propagation of statistical quantities in probabilistic power analysis.

9. Name the software sources that cause power dissipation.

10. List any two approaches towards software power estimation.

PART B — (5 × 16 = 80 marks)

11. (a) (i) What are the major factors that contribute to power dissipation in CMOS circuits? Explain how the reduction of these parameters influence power? (10)

(ii) Define the figure of merits of low power system or chip. (6)

Or

(b) With relevant expression, discuss the effects that influence the threshold voltage of MOS transistor.

12. (a) State the algorithm for power dissipation driven multilevel logic optimization and illustrate with an example.

Or

(b) (i) With example, explain the importance of transistor sizing in power dissipation. (8)

(ii) Explain the various power saving techniques for flip flops and latch circuits. (8)

13. (a) Describe the design of low power CMOS circuits using bus architecture approach.

Or

(b) Explain on clocked power reduction techniques with schematic.

14. (a) Discuss the technique for estimating power dissipation in sequential circuits.

Or

(b) Explain the statistical method of estimating average power in combinational logic circuits.

15. (a) How does operation reduction and operation substitution influence power optimization? Explain with example.

Or

(b) Describe the various methods can be used to minimize the software contribution to power dissipation.

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