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Reg. No. : | | | | | | | | | | | | |

Question Paper Code : 82443

M.E. DEGREE EXAMINATION, NOVEMBER/DECEMBER 2013.

Elective

Electronics and Communication Engineering

EC 9006/VL 9252/VL 952/10244 VLE 51 — LOW POWER VLSI DESIGN

(Common to M.E. VLSI Design and M.E. Applied Electronics and M.E. VLSI Design and Embedded Systems)

(Regulation 2009/2010)

Time : Three hours Maximum : 100 marks

Answer ALL questions.

PART A — (10 × 2 = 20 marks)

1. Why is CMOS technology preferred over other technologies for ICs?

2. What is short circuit power dissipation?

3. What are the effects of voltage scaling?

4. Write the importance of hierarchical clock gating.

5. List various computer arithmetic techniques for low power systems.

6. Write the techniques used for reducing power consumption in memories.

7. What is probabilistic power analysis? Mention its importance.

8. What are power estimation techniques?

9. What is synthesis?

10. Mention the need for low power VLSI design.

PART B — (5 × 16 = 80 marks)

11. (a) (i) Explain various sources of power consumption in CMOS. (8)

(ii) With usual notations show that the short circuit power dissipation in CMOS inverter is given by $P_{SC} = \beta / 12(V_{DD} - V_T)^3 \lambda / T$. (8)

Or

(b) Explain about the design limitations imposed on low-power, low voltage circuits pertaining to the following parameters.

(i) Power supply voltage

(ii) Threshold voltage

(iii) Scaling

(iv) Interconnect wires. (16)

12. (a) Explain circuit techniques for reducing power consumption in multipliers. (16)

Or

(b) Explain logical level power optimization techniques in detail. (16)

13. (a) Give the device structure and describe the fabrication process of low-voltage/low-power CMOS on SOI.

Or

(b) Write a short notes on :

(i) Junction isolation.

(ii) Collector-diffusion isolation.

(iii) LOCOS.

(iv) Shallow and Deeptreneh isolation. (16)

14. (a) Explain logic level power estimation techniques in detail. (16)

Or

(b) (i) Explain about optimization theme and performance theme of latches. (8)

(ii) What are the quality measures for latches and Flip-Flops? Explain. (8)

15. (a) Explain the software design techniques for low power IC design in detail. (16)

Or

(b) (i) Define signal gating. Explain the various logic implementation of signal gating. (12)

(ii) Write a note on body effect of long channel MOSFET. (4)
