Reg. No. : | | | | | | | | | | | | |

Question Paper Code : 11917

M.E. DEGREE EXAMINATION, NOVEMBER/DECEMBER 2014.

Elective

VLSI Design

VL 9252/EC 9006/VL 952/10244 VLE 51 — LOW POWER VLSI DESIGN

(Common to M.E. – Electronics and Communication M.E. – Applied Electronics)

(Regulation 2009/2010)

Time : Three hours Maximum : 100 marks

Answer ALL questions.

PART A — (10 × 2 = 20 marks)

1. What are the different sources of power consumption in CMOS circuits?

2. Define sub threshold swing.

3. What is Gate Delay Model?

4. What is optimization algorithm?

5. What is scaling interconnect?

6. How is power consumption reduced in memory?

7. Draw the flow chart of Monte-Carlo based technique for estimation of Average power in sequential circuits.

8. What is simulation power analysis?

9. Give error definition for CLS problem.

10. What are the sources of software power dissipation?

PART B — (5 × 16 = 80 marks)

11. (a) Explain in detail basic physics of power dissipation in CMOS FET devices.

Or

(b) Discuss in detail basic principle and limits of low power design.

12. (a) (i) How FSM helps in reducing power in Logic Level power optimization? Discuss. (8)

(ii) Explain how path conduction probability can be determined in CMOS gate model. (8)

Or

(b) With a neat circuit diagram explain how the power consumption can be reduced in adders and multipliers.

13. (a) Explain about computer arithmetic techniques available for low power system.

Or

(b) Describe about special techniques available for reducing power in CMOS circuits.

14. (a) Using signal probabilities derive the activities of static CMOS.

Or

(b) Explain about the techniques available to estimate glitching activity in logic circuits.

15. (a) Write short notes on :

(i) Power estimation using operation reduction and substitution (8)

(ii) Circuit Activity driven Architectural transformation. (8)

Or

(b) Explain in detail how software is optimized for low power.

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