Reg. No. | | | | | | | | | | | | |

Question Paper Code : 87273

M.E. DEGREE EXAMINATION, MAY/JUNE 2016

Second Semester

M.E. VLSI Design

VL 7202 – LOW POWER VLSI DESIGN

(Common to M.E. Applied Electronics)

(Regulations – 2013)

Time : Three Hours **Maximum : 100 Marks**

Answer ALL questions.

PART – A (10 × 2 = 20 Marks)

1. List out the limits of low power design.
2. Give the key principles of low power design.
3. What is Gate delay model ?
4. Discuss the phenomenon of the likelihood of state transition.
5. What are the four phases of operation in complementary adiabatic circuit ?
6. How will you reduce Glitch power ?
7. Define conditional probability.
8. What are the advantages of continuous signal model ?
9. What are the sources of software power dissipation ?
10. What is the need for synthesis of low power VLSI circuits ?

PART – B (5 × 13 = 65 Marks)

11. (a) (i) Explain in details basic principles of low power dissipation. (6)

(ii) Explain the dynamic power dissipation in CMOS inverter circuit and derive an expression for the same. (7)

OR

(b) Discuss elaborately the physics of power dissipation and power consumption in CMOS FET. (13)

12. (a) (i) Briefly discuss the pre-computational logic in power reconstruction in detail. (7)

(ii) Difference between area optimization and power optimization. (6)

OR

(b) (i) Explain logic level power optimization techniques in detail. (7)

(ii) Explain in detail the circuit level low power design. (6)

13. (a) Elaborate on any two techniques used to minimize power consumption in CMOS SRAM memories. (13)

OR

(b) Explain the computer arithmetic techniques for low power systems. (13)

14. (a) (i) Discuss the various power estimation techniques. (6)

(ii) Explain in detail probabilistic power analysis. (7)

OR

(b) Discuss the power estimation of CMOS combinational and sequential logic circuits using entropy. (13)

15. (a) How does software optimization lead to achieve low power ? Explain. (13)

OR

(b) Explain with suitable examples, the various transform applied at the behavioural level to realize low power circuits. (13)

PART – C (1 × 15 = 15 Marks)

16. (a) (i) With an example, explain the optimization procedure using operation reduction. What are its adverse effects ? **(8)**

(ii) With the aid of state transition diagram, discuss the state assignment algorithm that minimizes the activity and reduce power. **(7)**

OR

(b) (i) What are the special techniques available for reducing power ? Explain all the techniques. **(7)**

(ii) Power dissipation in a CMOS inverter is directly proportional to the load capacitance. Elaborate on this statement. **(8)**

———————