Reg. No. : | | | | | | | | | | | | |

Question Paper Code : 71873

M.E. DEGREE EXAMINATION, JUNE/JULY 2013.

Elective

VLSI Design

VL 9252/EC 9006/VL 952/10244 VLE 51 — LOW POWER VLSI DESIGN

(Common to M.E. Applied Electronics, M.E. Electronics and Communication Engineering and M.E. VLSI Design and Embedded Systems)

(Regulation 2009/2010)

Time : Three hours Maximum : 100 marks

Answer ALL questions.

PART A — ($10 \times 2 = 20$ marks)

1. Mention the different sources of power dissipation in CMOS technology.

2. Define work function.

3. Mention the parameters considered while developing performance-driven circuit optimization.

4. What are the state assignment problems associated with FSM?

5. Give the importance of clock signal for power optimized design in CMOS circuits.

6. What are tristate keeper circuits?

7. Distinguish between positive correlation and negative correlation.

8. Give the general model for sequential logic circuits.

9. Define voltage scaling technique for reducing power dissipation at architecture level.

10. What are reconfigurable computing?

PART B — (5 × 16 = 80 marks)

11. (a) (i) Starting from MOS physics derive an expression for the MOSFET threshold voltage. (11)

(ii) Mention the effect influencing threshold voltage in submicrometer MOSFET. (5)

Or

(b) (i) Discuss in detail about the basic principles of low power design. (11)

(ii) Distinguish between static and dynamic power consumption. (5)

12. (a) Explain about the logic level optimizations for low power in digital circuits. (16)

Or

(b) Describe about the different techniques adapted at circuit level for low power design. (16)

13. (a) Explain the various techniques used for reducing power consumption in RAM. (16)

Or

(b) Briefly explain about the power reduction techniques used in clock network. (16)

14. (a) Describe about the simulation power analysis at different abstraction level of VLSI. (16)

Or

(b) Explain about the role played by probability and statistics on reducing power consumption in digital circuits. (16)

15. (a) (i) Briefly explain about the algorithm level transforms for low power. (12)

(ii) Explain in detail about power optimization using operation reduction. (4)

Or

(b) Explain in detail about the software power optimization techniques with respect to instructions and memory accesses. (16)

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