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Question Paper Code : 11922

M.E. DEGREE EXAMINATION, NOVEMBER/DECEMBER 2014.

Elective

VLSI Design

VL 9257/VL 957/10244 VLE 41 — PHYSICAL DESIGN OF VLSI CIRCUITS

(Regulation 2009/2010)

Time : Three hours Maximum : 100 marks

Answer ALL questions.

PART A — (10 × 2 = 20 marks)

1. What is meant by logical design and physical design?
2. A chip is designed for implementing a new speech processing algorithm. The chip must be released into the market at a short deadline. What layout method will you use? Why?
3. What is cost function?
4. Define Assignment Problem.
5. Write the difference between Global routing and detailed routing.
6. State the significance of Steiner Tree.
7. How is delay minimization achieved in circuit layout?
8. State the limitations encountered in delay minimization.
9. What are Wein Burger arrays?
10. What are multichip modules?

PART B — (5 × 16 = 80 marks)

11. (a) (i) Explain with neat sketches teh layout rules in the design of VLSI circuits. (8)

(ii) With neat sketches explain the layout of standard cell gate arrays. (8)

Or

(b) (i) Explain with a neat diagram the steps involved in the design of Wein Nerger arrays. (8)

(ii) Describe the layout of FPGA with an example. (8)

12. (a) Explain the Kernighan-Lin partitioning algorithm with an example. (16)

Or

(b) (i) Write a note on floor plan sizing. (8)

(ii) Explain the simulated annealing based placement. (8)

13. (a) (i) Prove that the total weight of a minimum-spanning tree in an edge weighted graph is at most two times the length of an optimal Steiner tree in the same graph. (8)

(ii) Route the following channel consisting of 11 columns using the left edge algorithm where 0 indicates an empty position. (8)

TOP = 3 4 0 1 2 4 3 5 2 1 0

BOT = 1 0 3 0 4 0 5 2 1 5 4

Or

(b) (i) Briefly describe the various Steiner minimal Tree(SMT) algorithms used for global routing. (8)

(ii) Explain in detail about the routing in Array Based FPGAS and Row Based FPGAs. (8)

14. (a) Use the zero slack algorithm to find arrival time, required time and slacks in the circuit. Also explain how to use it to obtain a timing driven placement. (16)

Or

(b) (i) Using unconstrained via minimization technique show that any residual net can be routed with only one via. (8)

(ii) When would you use unconstrained via minimization and when constrained via minimization is more desirable? Explain. (8)

15. (a) Realize the following set of functions using a PLA with (16)

(i) Logic minimization alone

(ii) Folding alone

(iii) Logic minimization and folding.

$F1 = x_1 + x_2x_3x_4$

$F2 = x_1x_2x_4 + x_2x_3x_4x_5$

$F3 = x_1x_2 + x_2x_3 + x_1x_2$

$F4 = x_3x_4x_5 + x_2x_3$

Or

(b) Briefly explain how bend minimization can be minimized in single layer layout. (16)
