Reg. No. | | | | | | | | | | | | |

Question Paper Code : 18151

M.E. DEGREE EXAMINATION, NOVEMBER/DECEMBER 2016.

Elective

Applied Electronics

VL 7005 — PHYSICAL DESIGN OF VLSI CIRCUITS

(Common to M.E. VLSI Design)

(Regulations 2013)

Time : Three hours Maximum : 100 marks

Answer ALL questions.

PART A — (10 × 2 = 20 marks)

1. List out any two layout rules.
2. Define computational complexity.
3. What do you mean by partitioning?
4. Mention few algorithm that are used for floor planning.
5. Compare global and local routing.
6. State the merits and demerits of randomized routing.
7. What is meant by minimum steiner tree?
8. Highlight the issues in minimizing delay.
9. Distinguish global and detailed routing.
10. Why wire length should be minimized?

PART B — (5 × 13 = 65 marks)

11. (a) Describe Wien Berger arrays and Gate matrices. (13)

Or

(b) Explain layout of standard cells gate arrays and sea of gates. (13)

12. (a) Explain placement process using simulated annealing algorithm. (13)

Or

(b) How partition is done using Kerighan — Lin algorithm? (13)

13. (a) State the algorithm used for performing detailed routing and also explain it with an example. (13)

Or

(b) Explain the concept of maze routing with an example. (13)

14. (a) Explain about delay modeling concepts. (13)

Or

(b) Describe the various performance issues in circuit layout. (13)

15. (a) Define compaction and explain its types. (13)

Or

(b) Describe the significance of the cell routing. (13)

PART C — ($1 \times 15 = 15$ marks)

16. (a) Explain the routing architecture of FPGA. (15)

Or

(b) Define floor planning and how floor planning is performed in a physical circuit. (15)

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