Reg. No. : | | | | | | | | | | | | |

Question Paper Code : 64258

M.E. DEGREE EXAMINATION, NOVEMBER/DECEMBER 2015.

Elective

VLSI Design

VL 7005 — PHYSICAL DESIGN OF VLSI CIRCUITS

(Common to M.E. Applied Electronics)

(Regulations 2013)

Time : Three hours Maximum : 100 marks

Answer ALL questions.

PART A — (10 × 2 = 20 marks)

1. List some of the Layout rules of VLSI Circuits.
2. Draw the architecture of an array style EPGA.
3. Define Cost Function.
4. Write briefly about assignment problem.
5. Illustrate neatly the Top- down hierarchical routing approach.
6. What is Maze Running?
7. How clock skew can be reduced?
8. Define the characteristics of a Circle Graph.
9. Write down the steps involved in the OTC Routing.
10. Write briefly about the different types of algorithm available for 1-D compaction.

PART B — (5 × 16 = 80 marks)

11. (a) Describe in detail with necessary illustrations the different styles of layout available in the VLSI circuits. (16)

Or

(b) Assume there are seven items with sizes 1,4,2,1,2,3,5 and b = 6. A solution in this instance is to place the items with sizes 1 and 5 in one bin, those with sizes 2 and 4 in one bin, and the rest sizes 1,2, and 3 in the third bin. Find solution using Algorithmic Paradigm. (16)

12. (a) Enumerate in detail the algorithmic steps involved in the Ration cut Portioning with necessary expressions. (16)

Or

(b) What is Floor plan sizing? Explain in detail the Non-Hierarchical Floor plan sizing in the VLSI Circuits. (16)

13. (a) Describe with illustrations the construction and working principle of Minimum Length Steiner trees. (16)

Or

(b) (i) List out the steps involved in the Multi Commodity Flow algorithm. (8)

(ii) Describe in detail the Routing Architecture of the Row based FPGA's. (8)

14. (a) With neat sketch, Enumerate in detail the different types of delay model available in modeling of ICs. (16)

Or

(b) Discuss in detail the procedure involved in obtaining a Effective Timing-driven global router using delay minimizations. (16)

15. (a) Realize the following set of functions using PLAs. (16)

(i) Logic Minimization alone

(ii) Folding alone

(iii) Logic Minimization and Folding

F1 = x1+x2 x3 x4

F2 = x1 x2 x4 + x2 x3 x4 x5

F3 = x1 x3 + x2 x4 + x1 x2

F4 = x3 x4 x5 + x2 x3.

Or

(b) Explain in detail with neat diagram how the bend minimization can be reduced in the Single Layer Layout. (16)

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