Reg. No. | | | | | | | | | | | | |

Question Paper Code : 86349

M.E. DEGREE EXAMINATION, MAY/JUNE 2016

Elective

VLSI Design

CU7001 – REAL TIME EMBEDDED SYSTEMS

(Common to M.E. Biometrics and Cyber Security/M.E. Communication Systems, M.E. Communication and Networking/M.E. Electronics and Communities Engineering/M.E.Medical Electronics)

(Regulations 2013)

Time : Three Hours **Maximum : 100 Marks**

Answer ALL questions.

PART – A (10 × 2 = 20 Marks)

1. Mention the parameters used to evaluate the performance of the CPU.
2. List out the functional and nonfunctional requirements that needs to be satisfied by an embedded system.
3. Draw the stages in a four cycle handshake protocol.
4. What is meant by a symbol table ?
5. Distinguish between a task and a process.
6. What is context switching ?
7. Mention the necessity for a hardware accelerator in embedded system.
8. Draw the CAN data frame packet format.
9. What are the methods for testing a software modem ?
10. What do you understand by "feature creep" ?

PART – B (5 × 13 = 65 Marks)

11. (a) (i) Write the ARM assembly language for the following C statement :

for(i = 0, f = 0; i < N; i++)

f = f + c[i]*x[i]; **(7)**

(ii) With relevant examples, explain in detail about the event driven state machine for describing the behavior of a system. **(6)**

OR

(b) With neat diagrams, explain in detail about direct mapped cache organization and set associative cache organization. **(13)**

12. (a) (i) Explain the various debugging techniques used in embedded system design. **(7)**

(ii) Draw the state diagram of a bus bridge and explain it in detail. **(6)**

OR

(b) Explain in detail the compilation technique. **(13)**

13. (a) (i) With suitable examples, explain briefly about lightweight process and heavy weight process. **(6)**

(ii) Write a brief note on co-routine. **(7)**

OR

(b) Explain in detail about the power management and optimization for a process. Illustrate the basic global power states supported by Advanced Configuration and Power interface (ACPI). **(13)**

14. (a) Bring out the difference between single threaded and multithreaded control of an accelerator. With necessary sketches, explain briefly the system speedup evaluation for single threaded implementation and multithreaded implementation. **(13)**

OR

(b) Explain the bus arbitration scheme supported by Ethernet. Describe how an IP packet may be sent from a client on one Ethernet to a client on a second Ethernet. The two Ethernets are connected by a router. **(13)**

15. (a) With relevant diagrams, explain the hardware and software architecture of a personal digital assistant (PDA). **(13)**

OR

(b) (i) Write short notes on System on Silicon (SoS) and also illustrate the advantages and limitations of SoS. **(6)**

(ii) With the help of UML diagrams, mention the operation and functionalities supported by a data compressor. **(7)**

PART – C (1 × 15 = 15 Marks)

16. (a) (i) Bring out the difference between static scheduling and dynamic scheduling policies. **(4)**

(ii) Given the following set of periodic processes running on a single CPU, what is the maximum execution time for P5 for which all the processes will be schedulable using RMS ? **(6)**

Process	CPU time	Deadline
PI	1	10
P2	18	100
P3	2	20
P4	5	50
P5	X	25

(iii) Explain the application for FOSS tools for embedded system development. **(5)**

OR

(b) (i) Assume that a system has a two-level cache : The level 1 cache has a hit rate of 90% and the level 2 cache has a hit rate of 97%. The level 1 cache access time is 4 ns, the level 2 access time is 15 ns, and the level 3 access time is 80 ns. What is the average memory access time ? **(5)**

(ii) Assume an A/D converter is supplying samples at 44.1 kHz. If the interrupt handler executes 100 instructions obtaining the sample and passing it onto the application routine, how many instructions can be executed on a 20 MHz ARM processor that executes 1 instruction per cycle ? **(5)**

(iii) Explain briefly on internet enabled systems. **(5)**