Reg. No. | | | | | | | | | | | | |

**Question Paper Code : 86069**

**M.E. DEGREE EXAMINATION, MAY/JUNE 2016**

**Elective**

**Applied Electronics**

**AP7016 : SYSTEM ON CHIP DESIGN**

**(Common to M.E. VLSI Design)**

**(Regulations 2013)**

**Time : Three Hours** **Maximum : 100 Marks**

**Answer ALL questions.**

**PART – A (10 × 2 = 20 Marks)**

1. Why is there an inverter at the output of the domino gate ?
2. Define delay and transition delay.
3. What is charge sharing ?
4. How are Electrical effort and effort delay calculated ?
5. What are the sources of clock skew ?
6. Distinguish between latch and flip-flop.
7. Sketch the structure of a carry look ahead adder.
8. What are the types of memory ?
9. What are the three phases of floor planning ?
10. List the varieties of packages available.

## PART – B (5 × 13 = 65 Marks)

11. (a) (i) Illustrate with sketches why nMOS should be used as pull down device and pMOS as pull up device. (6)

(ii) Draw the static complementary gate and its stick diagram for 2 input NAND and NOR gates. (7)

**OR**

(b) Explain how delay is taken care in inductive interconnects. (13)

12. (a) (i) Exemplify the effect of transistor sizing on adder circuits. (6)

(ii) What is left edge algorithm? How this can be used to route a channel ? (7)

**OR**

(b) (i) Design a multiplexer with four data inputs and four select inputs. The two select bits s1, s0 and their complements are all fed into the switch network. (6)

(ii) Discuss on controllability and observability with an example. (7)

13. (a) (i) Construct SR type clocked flip-flop and explain. (6)

(ii) Elaborate the design of a traffic light controller. (7)

**OR**

(b) (i) Draw the block diagram for a four-bit counter with an LSSD scan chain. (6)

(ii) Explain how glitch reduction reduces power in CMOS circuits. (7)

14. (a) (i) Discuss the design of SRAM cell. (6)

(ii) Outline the organization of a PLA with a neat diagram. (7)

**OR**

(b) Explain the working of booth and Wallace tree multiplier with neat sketch. (13)

15. (a) (i) Discuss on the tips for floor planning design. (6)

(ii) Briefly explain on global routing. (7)

**OR**

(b) With a neat diagram, outline the I/O architecture and explain the pad design. (13)

## PART – C (1 × 15 = 15 Marks)

**(Application / Design / Analysis / Evaluation / Creativity / Case Study)**

16. (a) Design a 4 bit carry look ahead adder using static complementary circuit. (15)

**OR**

(b) Design a 4*4 array multiplier. Draw the basic building block using static complementary logic. (15)

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