Reg. No. : | | | | | | | | | | | | |

Question Paper Code : 13040

M.E. DEGREE EXAMINATION, NOVEMBER/DECEMBER 2014.

Elective

Applied Electronics

AP 7010 — DATA CONVERTERS

(Common to M.E. VLSI Design)

(Regulation 2013)

Time : Three hours Maximum : 100 marks

Answer ALL questions.

PART A — (10 × 2 = 20 marks)

1. Define Sampling time and holding time.
2. Mention the features of sampling switches.
3. What is the concept of switched capacitor filter?
4. What is the difference between cascade amplifier and cascode amplifier?
5. Enumerate the parameters of a DAC. Define them.
6. What is the significance of DAC and ADC ?
7. Which is the fastest ADC? Why?
8. What is the function of the successive approximation register in ADC?
9. What is the role of R_{OM} in Op amp? What does it signify?
10. Enumerate the typical parameters of Op amp.

PART B — (5 × 16 = 80 marks)

11. (a) (i) State and explain Miller effect.

(ii) Explain the principle of Sample and hold circuit with a neat diagram.

Or

(b) Explain the switched capacitor architecture with a neat diagram.

12. (a) (i) Explain the operation of switched capacitor amplifier with a circuit diagram.

(ii) Give an account on "Applications of switched capacitor integrator".

Or

(b) Explain the principle of cascaded amplifier stages with neat diagram.

13. (a) (i) Explain the concept of a simple DAC with a diagram.

(ii) Describe the switching and logic functions in DAC.

Or

(b) Explain in detail the current steering DAC architecture with a neat diagram.

14. (a) (i) Explain the flash ADC architecture and its features in detail.

(ii) Give an account on "Pipelined ADC architecture".

Or

(b) Explain the successive approximation architecture in detail with a neat diagram.

15. (a) Discuss the concept of op amp offset cancellation in detail ,with a neat diagram.

Or

(b) Write technical notes on:

(i) Calibration techniques

(ii) Comparator offset cancellation.

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