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Question Paper Code : 18160

M.E. DEGREE EXAMINATION, NOVEMBER/DECEMBER 2016.

Elective

VLSI Design

VL 7014 — IP BASED VLSI DESIGN

(Regulations 2013)

Time : Three hours Maximum : 100 marks

Answer ALL questions.

PART A — (10 × 2 = 20 marks)

1. Differentiate between ASIC and SoC.
2. Define body effect.
3. Draw the AND/NAND logic using DCVSL.
4. Find the logic effort of the 4 input nand gate.
5. Define clock skew.
6. Differentiate between bus and NoC.
7. What are H-tree and balanced tree in clock distribution networks?
8. List the major styles of GALS system.
9. State the functions of configurable CPU in IP based design.
10. What is Hard IP?

PART B — (5 × 13 = 65 marks)

11. (a) With a neat cross section of n-type MOS transistor, explain the operation of a transistor and also explain the transistor's behavior with necessary equations. (13)

Or

(b) (i) List out the fabrication errors that can occur during chip manufacture and explain. (8)

(ii) Draw the layout diagram of 2 input NOR gate. (5)

12. (a) (i) Realize the logic expression $Y = A'B' + C'D'$ in static complementary gates. (5)

(ii) Describe the working of Domino OR gate with neat diagrams. Why there is an inverter at the output of the domino gates. (8)

Or

(b) (i) List out the techniques of wiring optimization in combinational logic networks. Explain any two. (8)

(ii) Discuss the sources of glitching with a chain of adders. How can they be eliminated? (5)

13. (a) (i) Analyze the different clocking disciplines and clocking rules used in sequential logic networks. (9)

(ii) State whether the circuit shown in Fig 13(a) is a latch or edge triggered register. Justify your answer. (4)

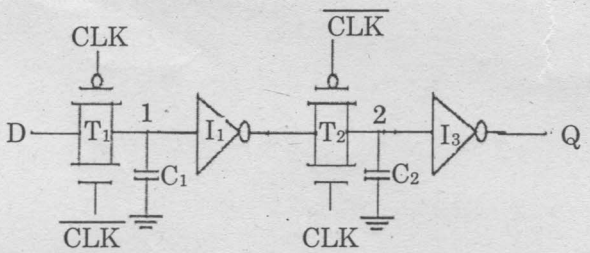

Fig. 13(a)

State the role of capacitances C1 and C2 and inverters.

Or

(b) (i) Design a four-bit Array multiplier and analyse the critical delay path in the circuit. (6)

(ii) Construct a 6T based SRAM cell. Explain its read and write operations. What are the role of sense amplifier in SRAM cells. (7)

14. (a) Explain the three phases of floor planning in detail with necessary diagrams.

Or

(b) Explain in detail about the low power architectural design techniques to reduce the power Consumption.

15. (a) Illustrate the design flow based on IP reuse in detail. Discuss the process of integrating IPs and doing physical chip design with procedural steps.

Or

(b) Explain the block diagram of the constraint based water marking technique with watermark embedding and signature verification procedures.

PART C — (1 × 15 = 15 marks)

16. (a) (i) Detect the faults mentioned in the circuit shown in Fig. 16(a)(i) to be tested one at a time by applying values for the primary inputs. (6)

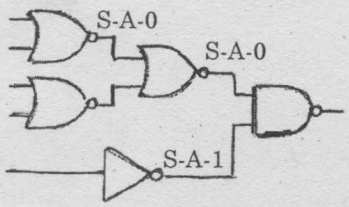

Fig. 16(a)(i)

(ii) Consider the circuit shown in Fig. 16(a)(ii). What is the logic function implemented by the CMOS transistor network? Size the transistors so that its pullup and pulldown times are approximately equal. (9)

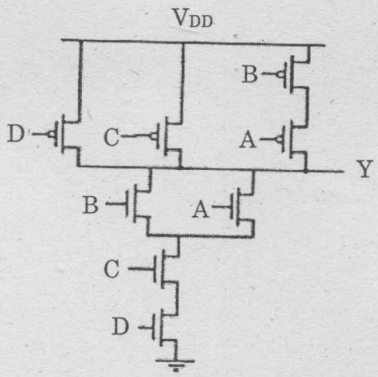

Fig. 16(a)(ii)

Or

(b) (i) Obtain the transition table and transition graph for a two-bit conditional counter. The counter has two inputs : 'count' increments the counter and reset' sets the value to 0. Its output is the counter value. Design the logic network.

(ii) Analyze the clock skew problems in flip flop based machines with the help of timing waveforms.