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Question Paper Code : 82135

M.E. DEGREE EXAMINATION, JUNE 2012.

Elective

VLSI Design

VL 9251/252071/VL 951/10244 VLE 22 — TESTING OF VLSI CIRCUITS

(Regulation 2009)

Time : Three hours Maximum : 100 marks

Answer ALL questions.

PART A — (10 × 2 = 20 marks)

1. Define fault coverage and effective fault coverage.

2. What are the various categories of manufacturing tests?

3. What is fault grading?

4. Give the sequence by which a sequential machine in tested.

5. Mention the common techniques involved is adhoc testing.

6. What are scan based test techniques?

7. How adaptive test generation for BIST in done? In what way this is efficient?

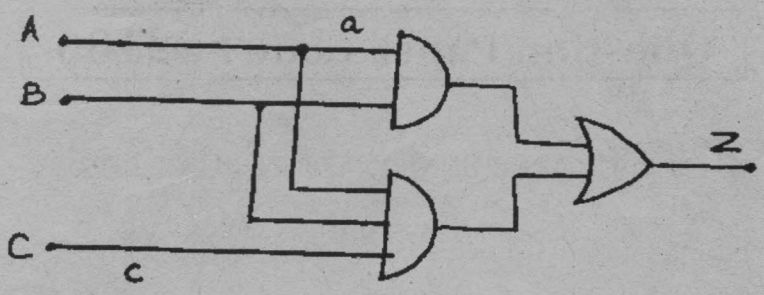
8. List the classification of off-line BIST Architecture.

9. State the limitation of using fault - dictionary approach for fault diagnosis.

10. What are the three assumptions made in developing a PMC model for diagonizing a system?

PART B — (5 × 16 = 80 marks)

11. (a) (i) For the circuit shown below :



Find the set of all tests that detect the fault 'c' s-a-1, fault 'a' s-a-0 and the multiple fault {'c' s-a-1, 'a' s-a-0}. (8)

(ii) Briefly describe the different delay models associated with the behaviour of the components in the event driven simulation. (8)

Or

(b) (i) Prove that in a combinational circuit, if two faults dominate each other, then they are functionally equivalent. Give an example. (8)

(ii) Prove that in an irredundant two-level combinational circuit, any complete test-set for SSFs also detects all multiple stuck-faults, with a case study. (8)

12. (a) (i) Show that a heuristic functional test, that does not detect a detectable stuck fault, cannot completely exercise its operation. (8)

(ii) Explain with an example how to detect all simple faults affecting the execution of any instruction. (8)

Or

(b) (i) Consider a gate level model of a 2 to 4 decoder. Show that any SSF leads to the following faulty behaviour : for any input vector, instead of, or in addition to the expected output line, some other output is activated, or no output is activated. (8)

(ii) Explain the text generation procedure for testing the register decoding function. (8)

13. (a) (i) Summarize the rules used for level-sensitive scan design. (8)

(ii) Write a brief note on system level DFT architecture. (8)

Or

(b) (i) Describe how partitioning large combinational circuits into small sub circuits and avoiding use of redundant logic reduce test generation cost of combinational circuit. (8)

(ii) Consider a random access scan architecture. How would you organize the test data to minimize the total test time? Describe a simple heuristic for ordering these data. (8)

14. (a) Explain with a typical design the circular self-test path BIST architecture in detail. (16)

Or

(b) Write a note on :

(i) Test pattern generation for BIST (8)

(ii) Embedded BIST architecture. (8)

15. (a) Illustrate with an example guided probe testing. Discuss the extention it needs to handle feedback loops, wired logic and speed up the diagnosis process. (16)

Or

(b) Prove that in a one-step t-fault diagnosable system, there must be atleast $2^t + 1$ units and each unit must be diagonized by atleast t other units. (16)
