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Question Paper Code : 71872

M.E. DEGREE EXAMINATION, JUNE/JULY 2013.

Elective

VLSI Design

VL 9251/VL 951/10244 VLE 22 – TESTING OF VLSI CIRCUITS

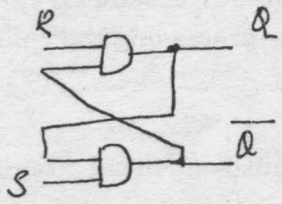
(Regulation 2009/2010)

Time : Three hours Maximum : 100 marks

Answer ALL questions.

PART A — (10 × 2 = 20 marks)

1. Draw a possible model for compiled simulation for the given Latch.



2. Find a circuit that has an undetectable stuck fault.

3. What is back tracking?

4. Define the D-frontier for the q-v algorithm.

5. What are the design values of LSSD network?

6. List out the attributes associated with the use of scan designs.

7. Which is the problem addressed by BIBLO?

8. In a CATSBIST architecture, why is it necessary that all storage cells be initialized to a known state before executing a test?

9. Define the basic guided probe procedure.

10. Consider a f-bit Hamming single-error correction code. For each of the following, assuming at most a single-bit error determine the erroneous bit if any 0101100, 0101101, 0111101.

PART B — (5 × 16 = 80 marks)

11. (a) For the given circuit (Fig. 11(a))

(i) Find the set of all tests that detect the fault a $s-a-o$.

(ii) Find the set of all tests that detect the fault b $s-a-o$.

(iii) Find the set of all tests that detect the multiple fault $\{a\ s-a-o, b\ s-a-o\}$.

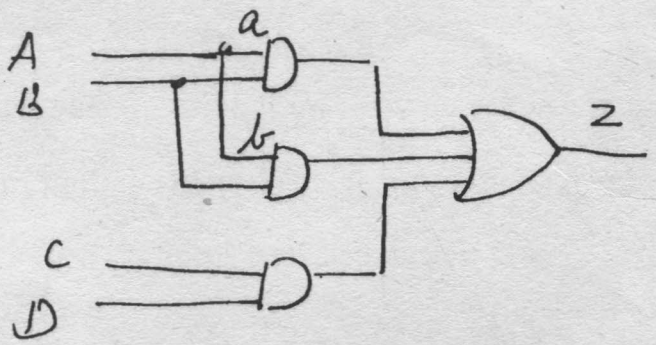


Fig. 11(a)

Or

(b) Draw the general structure for event-driven simulation with an algorithm and perform the activation of an already scheduled gate. Also design an algorithm with one pass strategy for processing the changes in multiple inputs.

12. (a) Generate test sequences for SSF in synchronous sequential circuits with JK flip flop using iterative array models.

Or

(b) Prove that the test set generated by using procedure CPTGFF for a fan out-free circuit is complete for SSFS.

13. (a) What is partial scan? How is it done using I paths? Show the structures and the logic block to be tested using I-path partial scan.

Or

(b) Consider a random-access scan architecture. How would you organize the test data to minimize the total test time? Describe a simple heuristic for ordering these data.

14. (a) How do you classify the off-line BIST architectures? What are the key elements of it? Explain with examples.

Or

(b) (i) Analyze the operation and performance of CEBS. (8)

(ii) What are the three phases involved in the testing of circular self-test path? Analyze the performance with a general form of design.

15. (a) Consider the following design of a (Fig. 15(a)) K-bit equality checker $(K \geq 3)$ to determine the equivalence of two words $(a_1, a_2, \ldots a_k)$ and $(a_1^1, a_2^1 \ldots a_k^1)$. The circuit has two outputs f_K and g_K defined by the recursive equations

$$f_K = f_{K-1} b_K + g_{K-1} a_K$$
$$g_K = f_{K-1} a_K + g_{K-1} b_K$$

where $b_K = \overline{a}_K^1$ and f_2 and g_2 are defined in the figure. Verify that this circuit is totally self-checking for all single stack fault?

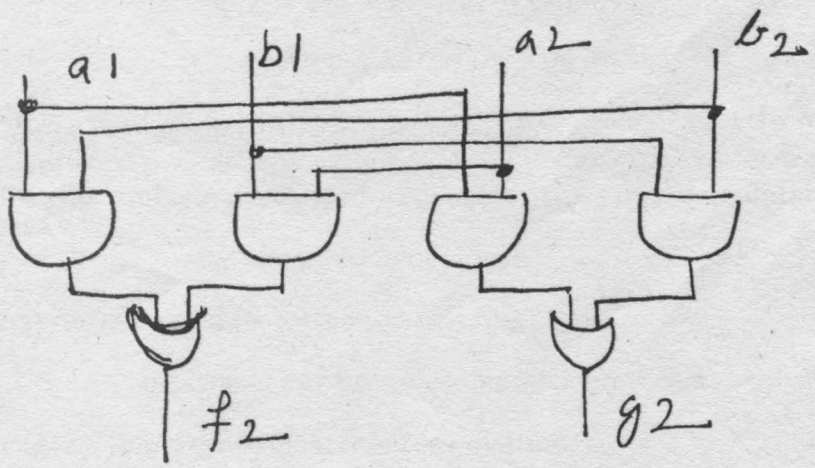


Fig. 15(a)

Or

(b) Consider a system whose diagnostic graph has five nodes $\{0,1,2,3,4\}$ and an edge from i to $(i+1) \bmod 5$ and from i to $(i+2) \bmod 5$ for all i.

(i) Prove that such a system is one-step two-fault diagnosable and sequentially two-fault diagnosable.

(ii) What is the maximum number of edges that can be removed from this graph so that it is still one-step two-fault diagnosable, or so that it is still sequentially two-fault diagnosable?
