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Question Paper Code : 14124

M.E. DEGREE EXAMINATION, NOVEMBER/DECEMBER 2014.

Third Semester

VLSI Design

VL 7301 — TESTING OF VLSI CIRCUITS

(Common to M.E. Applied Electronics)

(Regulation 2013)

Time : Three hours — Maximum : 100 marks

Answer ALL questions.

PART A — (10 × 2 = 20 marks)

1. State the two basic differences between combinational and sequential circuits.

2. What are the two basic steps in Test Generation using Path Sensitization method?

3. Give the expressions to compute the controllability and observability values for a T flip-flop with a synchronous clear input.

4. What do you mean by BIST?

5. Give the name of any two algorithms that is used for test pattern generation in Embedded RAMs.

6. State the need for Ad-hoc design in testing a digital circuit.

7. What do you mean by Pseudo-exhaustive test?

8. Draw the functional block diagram of TAP.

9. What are the Components in fault diagnosis?

10. What do you mean by dynamic diagnosis?

PART B — (5 × 16 = 80 marks)

11. (a) (i) Write a note on Event Driven simulation and explain what action an event-driven true-value simulator will take when it evaluates a zero-delay gate. (10)

(ii) Using functional fault modeling, determine the test sets for the following.

(1) An 8-line-to-1-line multiplexer (3)

(2) A 3-to-8 decoder. (3)

Or

(b) For a 2-input CMOS NAND circuit :

(i) Find a two-pattern test for each single-transistor stuck-open fault. (4)

(ii) Rearrange the eight vectors in a compact set, and show that this set can be constructed from the single stuck-at faults tests for the NAND gate. (4)

(iii) For each stuck-at fault of the NAND gate, find an equivalent transistor (stuck- open stuck-short or combination) fault. (8)

12. (a) For the combinational circuit shown in Figure 1, use the recursive algorithm (with propagate and justify functions) with D-algebra to determine the test vectors to detect the following faults :

(i) f stuck-at-0

(ii) h stuck-at-1

(iii) b stuck-at-0

(iv) b1 stuck-at-1.

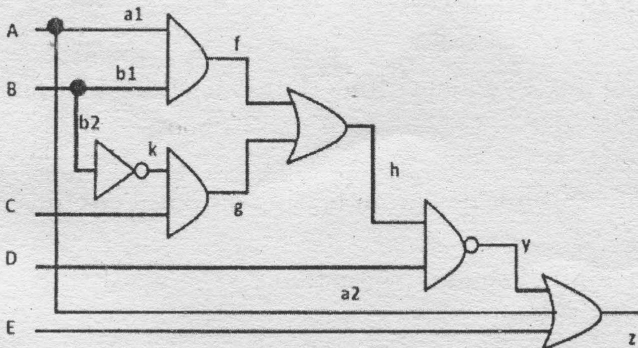

Figure 1

Or

(b) For the sequential circuit shown in Figure 2 use the Time-Frame Expansion method to detect the faults.

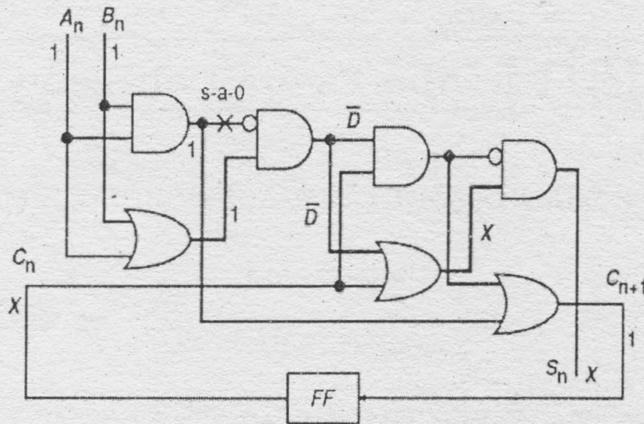

Figure 2

13. (a) Explain in detail about LSSD with example and justify how it is specifically used to scan paths in sensitive latches.

Or

(b) Discuss in detail about various DFT approaches used in testing a digital circuit.

14. (a) Explain in detail how an LFSR can be used as Pseudo-Random Pattern Generator. If N = 15 patterns are produced by an LFSR, and 2 of those patterns detect a given fault, say e stuck-at 0, what is the average test length T to detect e stuck-at-0?

Or

(b) With neat block diagram explain BIST architecture in detail.

15. (a) Explain in detail about the methods adopted for fault diagnosis in combinational circuits.

Or

(b) Discuss in detail how self checking method is adopted to test a circuit to diagnosis the fault.