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Question Paper Code : 18167

M.E. DEGREE EXAMINATION, NOVEMBER/DECEMBER 2016.

Third Semester

Applied Electronics

VL 7301 — TESTING OF VLSI CIRCUITS

(Common to M.E. VLSI Design)

(Regulations 2013)

Time : Three hours Maximum : 100 marks

Answer ALL questions.

PART A — (10 × 2 = 20 marks)

1. Define fault and list some faults that occur in digital circuits.
2. Mention some methods to detect fault in digital VLSI circuits.
3. Compare and contrast structural and functional test in test generation.
4. With the help of an example, illustrate the cyclic circuits.
5. Define Controllability and Observability.
6. Give the need for design for testing.
7. What is the role of LFSR in BIST?
8. Mention the principle of operation of circular BIST.
9. Mention the importance of fault dictionary in fault diagnosis.
10. What are self checking design?

PART B — (5 × 13 = 65 marks)

11. (a) Explain in detail about the different process involved in the fault modeling for combinational and sequential circuits.

Or

(b) Describe the process of gate level event driven simulation with an example.

12. (a) Illustrate the process of test generation for combinational logic circuits.

Or

(b) Describe in detail about the design of testable sequential circuits.

13. (a) By means of adding test and control points, explain the Adhoc design for testability techniques.

Or

(b) Explain about the full serial integrated, isolated serial and non serial scans of generic scan based design.

14. (a) Describe the different types of architectures involved in Built In Self Test methodology.

Or

(b) Discuss the different techniques used for designing testable memories.

15. (a) Explain the various process and steps involved in fault diagnosis at logic level.

Or

(b) With the help of an example illustrate the generalization of the PMC model for system level diagnosis.

PART C — (1 × 15 = 15 marks)

16. (a) Illustrate the application of PODEM algorithm using the logical circuit shown in Figure 16 (a). Derive two separate test vector for the circuit considering wire l with S-A-0 fault and S-A-1 fault.

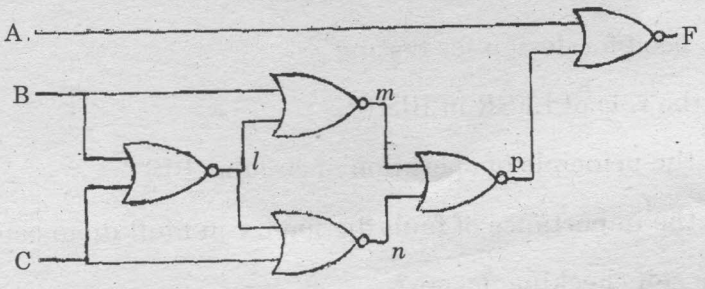

Figure 16 (a) Circuit under Test for PODEM algorithm

Or

(b) Construct a pseudo random sequence generator using the primitive polynomial $1 + x^2 + x^3$ with external XOR LFSR. Identify the proper seed value for the LFSR to get the maximal length Sequence.

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