Reg. No. : | | | | | | | | | | | | |

Question Paper Code : 91851

M.E. DEGREE EXAMINATION, JANUARY 2012.

Elective

VLSI Design

VL 9251 TESTING OF VLSI CIRCUITS

(Regulation 2009)

Time : Three hours **Maximum : 100 marks**

Answer ALL questions.

PART A — (10 × 2 = 20 marks)

1. How are stuck-at faults modeled in digital circuits?

2. What is the need for fault simulation?

3. Write down the propagation D Cube for a 3 input NAND gate.

4. How is homing sequence used in sequential circuit testing?

5. Give any two adhoc design rules?

6. Draw the logic structure of boundary scan cell.

7. Mention the various BIST architectures used in digital circuits.

8. List the fault models used in memory testing.

9. How is fault diagnosis performed in combinational circuits?

10. What is meant by self checking system?

PART B — (5 × 16 = 80 marks)

11. (a) (i) Explain fault equivalence and fault dominance. (8)

(ii) Write a note on Event-driven simulation. (8)

Or

(b) Discuss Deductive and concurrent fault simulation techniques with examples.

12. (a) Explain the scan path technique used in sequential circuit testing.

Or

(b) (i) Using Boolean difference method find the test vectors for the fault of 'S/O' in the given function. (10)

$F(a, b, c) = a'b'c + a'bc' + ab'c' + abc$.

(ii) In Boolean difference method explain how fault detection is possible even if the fault exists in internal lines. (6)

13. (a) Explain single latch and double latch LSSD design with neat diagrams.

Or

(b) Describe the modes of operation of boundary scan architecture.

14. (a) Explain the test pattern generation and signature analysis methods used in BIST architectures.

Or

(b) Explain March Test and GALPAT Test used in memory testing and also explain how pattern sensitive faults are tested.

15. (a) Discuss Fault diagnosis by WT reduction.

Or

(b) Explain the application of error detection and correcting codes in self checking design.

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