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Question Paper Code : 64274

M.E. DEGREE EXAMINATION, NOVEMBER/DECEMBER 2015.

Third Semester

VLSI Design

VL 7301 — TESTING OF VLSI CIRCUITS

(Common to M.E. Applied Electronics)

(Regulations 2013)

Time : Three hours Maximum : 100 marks

Answer ALL questions.

PART A — (10 × 2 = 20 marks)

1. Define controllability in digital circuits.

2. What is meant by delay modeling in logic gates?

3. List out the drawbacks encountered with random test generation for sequential circuits?

4. Relate the terms fault detection and fault location with fault diagnosis.

5. How sequential circuits are tested using scan path method?

6. Mention the common techniques involved in Adhoc testing.

7. List the types of coupling faults existing in memories.

8. What do you mean by Pseudo-exhaustive test?

9. State the limitation of using fault dictionary approach for fault diagnosis.

10. Enumerate the various features of on-line testing for fault detection.

PART B — (5 × 16 = 80 marks)

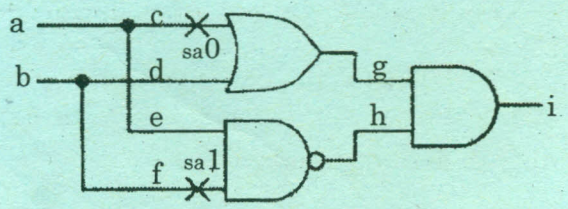
11. (a) (i) Write a note on event driven simulation and explain what action an event-driven true-value simulator will take when it evaluates a zero-delay gate. (8)

(ii) Explain in detail about any two fault detection technique in combinational logic circuit. (8)

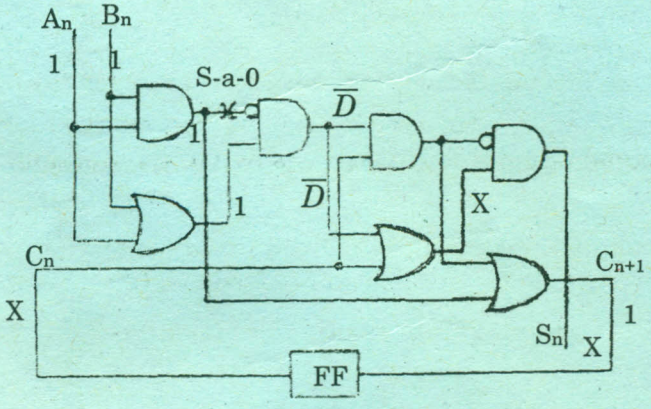
Or

(b) (i) Explain in detail about dominant fault collapsing with suitable example. (8)

(ii) Show that the two faults c s-a-0 and f s-a-1 are equivalent in the circuit of figure below. (8)



12. (a) (i) For the sequential circuit shown in figure, use the time-frame expansion method to detect the faults. (10)

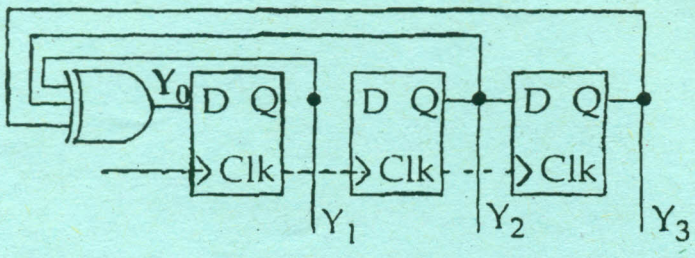


(ii) Explain PODEM algorithm. (6)

Or

(b) (i) Explain FAN algorithm with suitable logic circuit. (6)

(ii) Give the polynomial implemented by the following LFSR. Is it primitive? What is the length of the test sequence produced before repetition begins given the initial state of $Y_1Y_2Y_3 = 001$? (10)



13. (a) (i) Draw the LSSD latch logic diagram and show how these latches can be used in scan based designs. (8)

(ii) Discuss the Ad-hoc design methods used to improve the testability of circuits. (8)

Or

(b) (i) Discuss in detail about various DFT approaches used in testing a digital circuit. (8)

(ii) Describe how large combinational circuits partitioning into small sub-circuits with reduced test generation cost. (8)

14. (a) (i) Explain about GALPAT and Walking 0's and 1's concepts. (8)

(ii) Explain about test generations for Embedded RAMs. (8)

Or

(b) What are the different types of test pattern generators used in BIST architectures? Explain each of them with neat diagrams. (16)

15. (a) Discuss in detail about the fault diagnosis techniques used in combinational circuits and diagnosis by UUT reduction. (16)

Or

(b) Give one example for application of error-detecting and error-correcting codes and explain. (16)
