Reg. No. : | | | | | | | | | | | | |

Question Paper Code : 40991

B.E./B.Tech. DEGREE EXAMINATION, APRIL/MAY 2018
Third Semester
Electrical and Electronics Engineering
EE 6301 – DIGITAL LOGIC CIRCUITS
(Common to Electronics and Instrumentation Engineering/Instrumentation and Control Engineering)
(Regulations 2013)

Time : Three Hours | Maximum : 100 Marks

Answer ALL questions

PART – A **(10×2=20 Marks)**

1. State the associative property of Boolean algebra.
2. Reduce A(A + B).
3. Define duality property.
4. What is a karnaugh map ?
5. What is a master-slave flip-flop ?
6. Give the comparison between synchronous and asynchronous counters.
7. Define address and word.
8. Why was PAL developed ?
9. Define Cache memory.
10. Infer the concept of switch-level modeling.

PART – B **(5×13=65 Marks)**

11. a) i) Prove that $ABC + ABC' + AB'C + A'BC = AB + AC + BC$. **(8)**
ii) Convert the given expression in canonical SOP form $Y = AC + AB + BC$. **(5)**

(OR)

b) Designing a 4-bit Adder-Subtractor circuit. **(13)**

12. a) Write down the steps in implementing a Boolean function with levels of AND gates. **(13)**

(OR)

b) Give the general procedure for converting a Boolean expression in to multilevel NAND diagram. **(13)**

13. a) Explain the operation of SR flip-flop, T flip-flop and JK flip-flop. **(13)**

(OR)

b) Explain the flip-flop excitation tables for JK flip-flop and RS flip-flop. **(13)**

14. a) Elaborate the concept of PROM, EPROM, EEPROM in detail. **(13)**

(OR)

b) Explain the operation of bipolar RAM cell with suitable diagram. **(13)**

15. a) Give the different arithmetic operators and bitwise operators. **(13)**

(OR)

b) Explain in detail about the principal of operation of RTL design. **(13)**

PART – C **(1×15=15 Marks)**

16. a) Draw the circuit of CMOS AND gate and explain its operation. Also implement using PHDL. **(15)**

(OR)

b) Design and explain and bit shift register. Also give its truth table with its input and output waveform. **(15)**

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