Reg. No. : | | | | | | | | | | | | |

Question Paper Code : 21399

B.E./B.Tech. DEGREE EXAMINATION, MAY/JUNE 2013.

Fourth Semester

Electrical and Electronics Engineering

EE 2255/EE 46/EC 1261 A/10133 EE 406 A/080280029 — DIGITAL LOGIC CIRCUITS

(Regulation 2008/2010)

(Common to PTEE 2255 – Digital Logic Circuits for B.E. (Part-Time) Third Semester Electrical and Electronics Engineering – Regulation 2009)

Time : Three hours Maximum : 100 marks

Answer ALL questions.

PART A — (10 × 2 = 20 marks)

1. Construct OR gate using only NAND gates.

2. Define multiplexer.

3. Draw truth table for JK flipflop.

4. How many flip flops are required to design mod 25 counter?

5. What is the difference between flow table and transition table?

6. Define Race conditions in Asynchronous sequential circuit.

7. What is the difference between PROM and EPROM?

8. What are the advantages of CMOS?

9. Write HDL behavioural model of D flip flop.

10. What is the need for VHDL?

PART B — (5 × 16 = 80 marks)

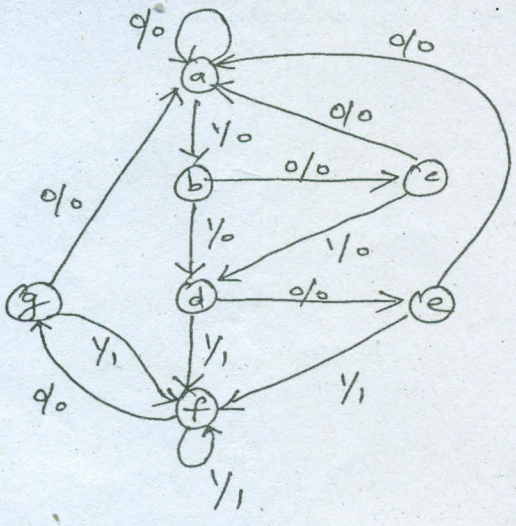
11. (a) (i) Prove that $F=\overline{A}\cdot B+A\cdot\overline{B}$ is exclusive OR operation and it equals $=\overline{\overline{(A\cdot B)}\cdot A}\cdot\overline{\overline{(A\cdot B)}\cdot B}$. (8)

(ii) Prove that for constructing XOR from NANDs we need four NAND gates. (8)

Or

(b) Simplify the Boolean function using Kmap $F(w,x,y,z)=\Sigma(1,3,7,11,15)$. which has the don't care conditions $d(w,x,y,z)=\Sigma(0,2,5)$.

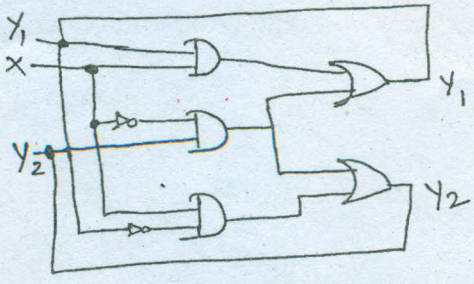
12. (a) Construct reduced state diagram for the following state diagram.



Or

(b) Design a 3 bit binary counter using T flip flop.

13. (a) Consider the following asynchronous sequential circuit and draw maps and transition table, and state table.



Or

(b) Illustrate the analysis procedure of asynchronous sequential circuit with an example.

14. (a) Illustrate the basic principles of PLA and FPGA.

Or

(b) Explain the basic working principles of TTL and ECL logic families.

15. (a) Write HDL for four bit binary counter with parallel load and explain.

Or

(b) (i) Write HDL for two to one line multiplexer with data flow description and behavioural description. (8)

(ii) Write HDL for four bit adder. (8)
