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Question Paper Code : 91442

B.E./B.Tech. DEGREE EXAMINATION, NOVEMBER/DECEMBER 2014.

Fourth Semester

Electrical and Electronics Engineering

EE 2255/EE 46/EC 1261 A/080280029/10133 EE 406 A — DIGITAL LOGIC CIRCUITS

(Regulation 2008/2010)

(Common to PTEE 2255/ 10133 EE 406 — Digital Logic Circuits for B.E (Part-Time) Second /Third Semester – EEE — Regulation 2009/2010)

Time : Three hours Maximum : 100 marks

Answer ALL questions.

PART A — (10 × 2 = 20 marks)

1. Draw the logic diagram of an half adder.

2. What are the applications of multiplexer?

3. Implement T flip flop using JK flip flop.

4. Define state.

5. What are the disadvantages of asynchronous sequential circuit?

6. Define racing.

7. How to program and erase the contents of EPROM?

8. What is advantages of ECL over TTL?

9. List out the operators used in VHDL.

10. What is a test bench?

PART B — (5 × 16 = 80 marks)

11. (a) (i) State and prove De-Morgan's theorem. (6)

(ii) Simplify the following Boolean expression using k-map $f(x,y,z)=\bar{x}\,\bar{y}z+xyz+xy\bar{z}+x\bar{y}z+x\bar{y}\bar{z}$. (5)

$$f(A,B,C,D)=\sum(0,1,5,6,7,10,12,14)+\sum_{d}(3,9).$$ (5)

Or

(b) (i) Draw the logic diagram of a 4 bit carry look ahead adder and explain how this adder is advantageous over the ripple carry adder. (10)

(ii) Explain with a suitable example how a muliplexer is used to implement the Boolean functions. (6)

12. (a) (i) Implement a clocked JK flip flop using NAND gates and explain its operation using a timing diagram. (10)

(ii) Implement D and T FFS using JK flip flop. Write down the characteristics equation of the three flip flop. (6)

Or

(b) (i) Draw the logic diagram of 4 bit synchronous counter. Explain the operation of the counter using the timing diagram. (8)

(ii) Explain the universal shift register in detail. (8)

13. (a) (i) Draw the ASM chart and explain how to anylse an asynchronous sequential machines. (10)

(ii) Discuss in detail the hazards and races in asynchronous sequential logic circuits. (6)

Or

(b) (i) What is meant by state transition diagram? Explain how state assignment is important in a sequential circuit design. Give a suitable example. (10)

(ii) What are the main considerations in an asynchronous sequential logic circuit design? Explain with a suitable example. (6)

14. (a) (i) Draw the hierarchy of memories based on the various features such as read/write access, speed, size of memory etc. Explain. (8)

(ii) Write short notes on EPROM. (8)

Or

(b) (i) Explain in detail how FPGA is used for implementation of a logic circuit. (8)

(ii) Write a detailed note on CMOS logic family. (8)

15. (a) (i) Explain in detail the various programming constructs used in VHDL for designing a logic circuit. (8)

(ii) Discuss the various packages. Write a VHDL code for the implementation of a decoder /demultiplexer. (8)

Or

(b) (i) Write a VHDL code for 4 bit synchronous up/down counter and explain. (10)

(ii) Write short notes on subprograms used for implementation of adders. (6)
