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Question Paper Code : 40483

B.E./B.Tech. DEGREE EXAMINATIONS, NOVEMBER/DECEMBER 2021.

Third Semester

Electrical and Electronics Engineering

EE 8351 – DIGITAL LOGIC CIRCUITS

(Common to B.E. Electronics and Instrumentation Engineering/
B.E. Instrumentation and Control Engineering)

(Regulations 2017)

Time : Three hours Maximum : 100 marks

Answer ALL questions.

PART A — ($10 \times 2 = 20$ marks)

1. Convert (9B2.1A)H to its binary equivalent.

2. List any four parameters that determine the characteristics of TTL logic family.

3. What is the difference between half adder and full adder?

4. Define shift registers.

5. Convert JK flipflop to D flip flop.

6. What are the different types of shift registers?

7. What is programmable logic array? How it differs from ROM?

8. What are the steps for the design of asynchronous sequential circuit?

9. What is verilog?

10. What is the structural gate level modeling?

PART B — ($5 \times 13 = 65$ marks)

11. (a) Explain the characteristics and implementation of the digital family ECL.

Or

(b) Write a note on CMOS characteristics.

12. (a) Obtain the minimum SOP using Karnaugh map method.

$F = m_0 + m_2 + m_4 + m_8 + m_9 + m_{10} + m_{11} + m_{12} + m_{13}$

Or

(b) (i) Implement a full adder circuit using decoder and using multiplexer.

(ii) Design a 2 bit magnitude comparator.

13. (a) Design a mod 6 counter using FFS. Draw the state transition diagram of the same.

Or

(b) Design a sequential circuit with 4 flipflops ABCD. The next states of B,C,D is equal to the present states of A, B, C respectively. The next state of A is equal to the EXOR of present states of C and D.

14. (a) Describe the concept and working of PLA

Or

(b) Describe the concept, working and application of FPGA.

15. (a) Write a VHDL program for 4 bit counter - Behavioral.

Or

(b) Write a VHDL program of Demultiplexer 1×4.

PART C — ($1 \times 15 = 15$ marks)

16. (a) Find the minimal SOP form for the following 6 variable switching function. $f(x_1, x_2, x_3, x_4, x_5, x_6) = \sum m(2, 3, 6, 7, 10, 14, 18, 19, 22, 23, 27, 37, 42, 43, 45, 46, 58, 59)$.

Implement the reduced function using NAND gates only.

Or

(b) A sequential circuit has one flip flop Q, two inputs x and y and one output S. It consists of a full adder circuit connected to a 'D' flip flop as shown below.

Derive the state table and state diagram of the sequential circuit.