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**Question Paper Code : 71637**

M.E. DEGREE EXAMINATION, JUNE/JULY 2013.

Second Semester

Power Electronics and Drives

PE 9224/PE 924 — MICROCONTROLLER AND DSP BASED SYSTEM DESIGN

(Common to M.E. High Voltage Engineering)

(Regulation 2009)

Time : Three hours

Maximum : 100 marks

Answer ALL questions.

PART A — (10 × 2 = 20 marks)

1. What are RISC and CISC processors?
2. What are the various addressing modes in PIC 16C7X processor?
3. What is watchdog timer?
4. What do you mean by the prescaling of PIC timers?
5. Write the different names of memory available in TMS320F24X digital signal processor.
6. What are the different buses of TMS320F24X?
7. What are the general purpose I/O pins in TMS320F24X DSP?
8. What is meant by A/D noise?
9. Distinguish between sine PWM and space vector PWM method.
10. What are the advantages of using DSP for speed control?

PART B — (5 × 16 = 80 marks)

11. (a) Discuss the architecture of PIC16C7X microcontroller with block diagram.

Or

- (b) (i) Write assembly language program for extended-precision subtraction and for integer multiplication with PIC16C7X microcontroller. (12)
- (ii) Explain any two addressing modes of PIC16C7X microcontroller with examples. (4)
12. (a) Discuss the interrupt structure in PIC microcontrollers and explain various interrupts of PIC 16C7X.

Or

- (b) Discuss different categories of PIC 16C7X timers in detail.
13. (a) Explain the architecture of TMS320F24X Processor with block diagram.

Or

- (b) Explain the following with respect to TMS320F24X family digital signal processor.
- (i) System configuration registers. (4)
- (ii) Pipelining operation (4)
- (iii) Addressing modes. (8)
14. (a) Write short note on the following with respect to DSP.
- (i) ADC (8)
- (ii) Event manager. (8)

Or

- (b) Explain various interrupts of TMS320F24X digital signal processor.
15. (a) Discuss the operation of microcontroller based speed control of DC shunt motor.

Or

- (b) Explain how SVPWM is implemented using DSP for speed control of inverter fed induction motor drive system.