Reg. No. | | | | | | | | | | | | |

Question paper Code: X11321

B.E./B.Tech. DEGREE EXAMINATIONS APRIL / MAY 2021

Second Semester

Artificial Intelligence and Data Science

AD8252 - DIGITAL PRINCIPLES AND COMPUTER ORGANIZATION

(Common to Computer Science and Data Science)

(Regulations 2017)

Time : 3 Hours | Answer ALL Questions | Max. Marks: 100

PART-A (10 x 2 = 20 Marks)

1. State De Morgan's theorem for three variables.
2. Find the dual of function $F = x\,(y'z' + yz)$.
3. What is overflow in binary arithmetic?
4. Draw 4x16 decoder using two 3x8 decoders.
5. What are little-endian and big-endian method of data storage?
6. How does a processor differentiate between opcode and data.
7. Differentiate between microprogrammed and hardwired control units.
8. Justify the need of pipelining in a processor.
9. What is the need of replacement algorithms in memory management?
10. Specify the address and data bus width of 64K x 8 memory chip. Justify the answer.

Part – B (5 x 13 = 65 marks)

11. a) i) Simplify $F(A,B,C,D) = \sum(0,1,2,5,8,9,10)$ in sum of product and product of sum form by using K-map. (6)

ii) Simplify the following Boolean expression by using K-map and draw the logic diagram for the simplified expression. (7)

$$F(A,B,C,D) = \sum(0,6,8,13,14)\ and\ d(A,B,C,D) = \sum(2,4,10).$$

OR

b) i) Simplify $F(A,B,C,D) = AC'D' + C'D + AB' + ABCD$ in sum of product and product of sum forms by using K-map. (6)

ii) Simplify the following Boolean expression by using K-map and draw the logic diagram for the simplified expression. (7)

$$F = AB'C + B'C'D' + BCD' + ACD' + A'B'C + A'BC'D$$

12. a) Design a four bit carry lookahead adder. (13)

OR

b) Design 32 to 1 multiplexer using four 8 to 1 multiplexer and 2 to 4 decoder. (13)

13. a) Explain the general addressing modes with examples. (13)

OR

b) Explain the basic operation of a processor with different stages of instruction execution. (13)

14. a) What are hazards in a pipelining? Explain different types of pipeline hazards with solutions? (13)

OR

b) Explain the data path of a processor that supports the basic type of instructions. (13)

15. a) Explain various cache mapping techniques in detail. (13)

OR

b) i) What is the role of a DMA controller in a processor-based system design. (7)

ii) What is an interrupt? Explain the interrupt-driven data transfer between processor and an IO device. (6)

PART C (1 X 15 = 15)

16. a) Implement the Boolean function $F(A,B,C) = \sum(0,1,4,6)$ by using

multiplexer

(i) Using A as input (15)

(ii) Using B as input

(iii) Using C as input.

Explain the design procedure in detail.

OR

b) Construct 2Mx32 bit memory by using 512Kx8 bit memory chips and a decoder. Illustrate the design with a neat diagram and explain it in detail. (15)