JANSONS INSTITUTE OF TECHNOLOGY

(Autonomous)

Accredited by NAAC 'A Grade' and ISO 9001: 2015 Certified Institution
Approved by AICTE and Affiliated to Anna University
Coimbatore – 641 659, Tamil Nadu, India.

M.E. VLSI Design and Embedded Systems

Curriculum and Syllabi

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Regulations 2024
Choice Based Credit System
M.E. VLSI Design and Embedded Systems
Curriculum and Syllabi for Semesters I and II

Semester - I

Sl. No.	Course Code	Course Title	Category	Periods per Week			Contact Hours	Credits
				L	T	P		
Theory Course								
1	P24VE1101	Graph Theory and Optimization Techniques	FC	3	1	0	4	4
2	P24CD4101	Research Methodology and IPR	RM	2	0	0	2	2
3	P24VE2101	Embedded Controllers	PC	3	0	0	3	3
4	P24VE2102	Embedded System Design	PC	3	0	0	3	3
5		Audit Course – I*	AC	2	0	0	2	0
Theory cum Laboratory Course								
6	P24VE2103	Digital CMOS VLSI Design	PC	3	0	2	5	4
7	P24VE2104	FPGA System Design	PC	3	0	2	5	4
Practical Courses								
8	P24VE2105	Embedded Systems Laboratory	PC	0	0	4	4	2
			Total	**19**	**1**	**8**	**28**	**22**

***Audit course is optional**

Semester – II

Sl. No.	Course Code	Course Title	Category	Periods per Week			Contact Hours	Credits
				L	T	P		
Theory Course								
1	P24VE2201	Design for Verification using UVM	PC	3	0	0	3	3
2	P24VE2202	Embedded Automation	PC	3	0	0	3	3
3	P24VE2203	VLSI Structures for DSP	PC	3	0	0	3	3
4	P24VE2204	Internet of Things System Design	PC	3	0	0	3	3
5		Professional Elective I	PE	3	0	2	5	4
6		Audit Course – II*	AC	2	0	0	2	0
Theory cum Laboratory Courses								
7	P24VE2205	Analog IC Design	PC	3	0	2	5	4
Practical Courses								
8	P24VE2206	Embedded Automation Laboratory	PC	0	0	4	4	2
			Total	**20**	**0**	**8**	**28**	**22**

***Audit course is optional**

PROFESSIONAL ELECTIVES
SEMESTER II, ELECTIVE I

Sl. No.	Course Code	Course Title	Category	Periods per Week			Contact Hours	Credits
				L	T	P		
Theory Course								
1	P24VE3201	Real Time Operating System	PE	3	0	2	5	4
2	P24VE3202	Embedded Networking	PE	3	0	2	5	4
3	P24VE3203	Deep Learning	PE	3	0	2	5	4
4	P24VE3204	Real Time Embedded Systems	PE	3	0	2	5	4
5	P24VE3205	Pervasive Computing	PE	3	0	2	5	4
6	P24VE3206	Physical Design Automation	PE	3	0	2	5	4

AUDIT COURSES (AC)

Registration for any of these courses is optional to students

Sl. No.	Course Code	Course Title	Category	Periods per Week			Contact Hours	Credits
				L	T	P		
Theory Course								
1	P24AC7001	English for Research Paper Writing	AC	2	0	0	2	0
2	P24AC7002	Disaster Management	AC	2	0	0	2	0
3	P24AC7003	Constitution of India	AC	2	0	0	2	0
4	P24AC7004	நற்றமிழ் இலக்கியம்	AC	2	0	0	2	0

P24VE1101	GRAPH THEORY AND OPTIMIZATION TECHNIQUES	L	T	P	C
		3	1	0	4

Course Objectives:	Introduce graph theory for connectivity problem-solving and fundamental algorithms. Teach real-life linear and non-linear programming for resource-constrained engineering and business, covering simulation modeling applications

Unit - I	GRAPHS	12

Graphs and graph models – Graph terminology and special types of graphs – Matrix representation of graphs and graph isomorphism – Connectivity – Euler and Hamilton paths.

Unit - II	GRAPH ALGORITHM	12

Graph Algorithms – Directed graphs – Some basic algorithms – Shortest path algorithms – Depth – First search on a graph – Theoretic algorithms – Performance of graph theoretic algorithms – Graph theoretic computer languages.

Unit - III	LINEAR PROGRAMMING	12

Formulation – Graphical solution – Simplex method – Two-phase method – Transportation and Assignment Models.

Unit – IV	NON-LINEAR PROGRAMMING	12

Constrained Problems – Equality constraints – Lagrangian Method – Inequality constraints – Karush – Kuhn-Tucker (KKT) conditions – Quadratic Programming.

Unit - V	SIMULATION MODELLING	12

Monte Carlo Simulation – Types of Simulation – Elements of Discrete Event Simulation – Generation of Random Numbers – Applications to Queuing systems.

Total Periods:	60

Course Outcomes

On completion of the course, the student can

CO	Statements	K-Level
CO1	Identify the special types of graphs, matrix representation of graphs and graph isomorphism.	K3
CO2	Make use of the fundamental graph algorithms to optimize the real-world issues.	K3
CO3	Construct a linear programming problem and utilize it to solve transportation and assignment problems.	K3
CO4	Solve the nonlinear programming problem using optimization techniques.	K3
CO5	Apply the simulation modeling techniques to solve the physical problems.	K3

Knowledge Level: K1 – Remember, K2 – Understand, K3 – Apply, K4 – Analyze, K5 – Evaluate, K6 – Create

CO – PO Articulation Matrix

	Programme Outcomes		
	01	**02**	**03**
CO1	3	2	2
CO2	2	2	2
CO3	3	2	3
CO4	2	3	3
CO5	2	2	3
CO	**2**	**2**	**3**

Correlation levels 1, 2 and 3 are as defined below:

1. Slight 2. Moderate 3. Substantial (High)

Reference Books

1	Taha H.A, "Operation Research: An Introduction", Ninth Edition, Pearson Education, New Delhi, 2010.
2	Gupta P. K, and Hira D.S., "Operation Research", Revise Edition, S. Chand and Company Ltd., 2012.
3	Douglas B. West, "Introduction to Graph Theory", Pearson Education, New Delhi, 2015.
4	Narasingh Deo, "Graph Theory with Applications to Engineering and Computer Science", Prentice Hall India,1997.
5	Sharma J.K., "Operation Research", 3rd Edition, Macmillan Publishers India Ltd., 2009.
6	Balakrishna R., Ranganathan. K., "A text book of Graph Theory", Springer Science and Business Media, New Delhi, 2012.
7	Reuven Y. Rubinstein and Dirk P. Kroese, "Simulation and the Monte Carlo Method", 3rd Edition, John Wiley & Sons, Hoboken, New Jersey, 2017.

P24CD4101	RESEARCH METHODOLOGY AND IPR	L	T	P	C
		2	0	0	2

Course Objectives:	To understand and familiarize with search problems, process and design, data collection, preparing process, statistical concepts in data analysis and reporting. To gain knowledge about statistical concepts in data analysis and reporting, intellectual property rights and its practices, patent rights and agents.

Unit - I	**RESEARCH DESIGN**	**6**

Overview of research process and design, Use of Secondary and exploratory data to answer the research question, Qualitative research, Observation studies, Experiments and Surveys.

Unit - II	**DATA COLLECTION AND SOURCES**	**6**

Measurements, Measurement Scales, Questionnaires and Instruments, Sampling and methods. Data - Preparing, Exploring, examining and displaying.

Unit - III	**DATA ANALYSIS AND REPORTING**	**6**

Overview of Multivariate analysis, Hypotheses testing and Measures of Association. Presenting Insights and findings using written reports and oral presentation.

Unit – IV	**INTELLECTUAL PROPERTY RIGHTS**	**6**

Intellectual Property – The concept of IPR, Evolution and development of concept of IPR, IPR development process, Trade secrets, utility Models, IPR & Biodiversity, Role of WIPO and WTO in PR establishments, Right of Property, Common rules of IPR practices, Types and Features of IPR Agreement, Trademark, Functions of UNESCO in IPR maintenance.

Unit - V	**PATENTS**	**6**

Patents – objectives and benefits of patent, Concept, features of patent, Inventive step, Specification, Types of patent application, process E-filing, Examination of patent, Grant of patent, Revocation, Equitable Assignments, Licences, Licensing of related patents, patent agents, Registration of patent agents.

	Total Periods:	**30**

Course Outcomes

On completion of the course, the student can

COs	Statements	K-Level
CO1	Outline the research process and its design.	K2
CO2	Apply the various methods for data collection and sources.	K3
CO3	Build data analysis and reporting methods for multivariate analysis.	K3
CO4	Explain the concepts of intellectual property rights and its practices.	K2
CO5	Summarize the concepts of patents.	K2

Knowledge Level: K1 – Remember, K2 – Understand, K3 – Apply, K4 – Analyze, K5 – Evaluate, K6 – Create

CO – PO Articulation Matrix

	Programme Outcomes		
	01	**02**	**03**
CO1	3	2	2
CO2	2	1	2
CO3	3	2	2
CO4	2	1	3
CO5	2	2	3
CO	**2**	**2**	**2**

Correlation levels 1, 2 and 3 are as defined below:

1. Slight 2. Moderate 3. Substantial (High)

Reference Books

1	Cooper Donald R, Schindler Pamela S and Sharma JK, "Business Research Methods", Tata McGraw Hill Education, 11e (2012).
2	Catherine J. Holland, "Intellectual property: Patents, Trademarks, Copyrights, Trade Secrets", Entrepreneur Press, 2007.
3	David Hunt, Long Nguyen, Matthew Rodgers, "Patent searching: tools & techniques", Wiley, 2007.
4	The Institute of Company Secretaries of India, Statutory body under an Act of parliament, "Professional Programme Intellectual Property Rights, Law and practice", September 2013.

P24VE2101	EMBEDDED CONTROLLERS	L	T	P	C
		3	0	0	3

Course Objectives:	To study the architecture and programming of PIC microcontrollers and to learn interfacing with them. To understand the ARM processor architecture and program using the ARM Instruction Set. Additionally, to design and develop embedded applications.

Unit - I	**PIC MICROCONTROLLER – ARCHITECTURE**	**9**

RISC Vs CISC Architectures – PIC Architecture and Assembly Language Programming - Program Memory Organization- Branch, Call and Time Delay Loop - PIC I/O Port Programming - Arithmetic and Logic Instructions and Programs - PIC Bank Switching, Table Processing, Macros And Modules PIC Configuration Registers-PIC Hardware Connection-ROM Loaders.

Unit - II	**PIC INTERFACING**	**9**

PIC Timer / Counter Programming - Timers 0 And 1- Programming Timers 2 and 3 -Serial Port Programming -Interrupt Programming -Flash / EEPROM Programming - Standard and Enhanced CCP Modules -Compare Mode Programming - Capture Mode Programming- PWM Programming- ECCP Programming.

Unit - III	**ARM ARCHITECTURE**	**9**

Introduction to ARM Processor families – Pipeline- ARM7TDMI Programmers Model- Processor Modes-Program Status Registers - Vector Table- Assembler Rules and Directives - Predefined Register Names – Macros – Assembler – Operators – Literals - Load and Store Instructions - Operand Addressing – Endianness - Arm Rotation Scheme - Loading Constants and Addresses into Registers.

Unit – IV	**ARM PROGRAMMING**	**9**

ARM Instruction Set - Data Processing Instructions – Branch Instructions — Load Store Instructions – Software Interrupt Instruction – Program Status Register Instructions – Conditional Execution - Thumb Instruction Set-Thumb Programmers Model-Thumb Branch Instructions- Thumb Data Processing Instructions-Thumb Single Register Data Transfer- Thumb Multiple Register Data Transfer Instructions - Thumb Implementation.

Unit - V	**EMBEDDED APPLICATIONS**	**9**

ADC, DAC and Sensor Interfacing –LCD and Keyboard Interfacing -Calculator with Keypad – Relays and Optoisolators - Stepper Motor Interfacing - DC Motor Interfacing - PWM Motor Control with CCPDC - Motor Control With ECCP.

	Total Periods:	**45**

Suggested Activities

1. Interfacing PIC microcontrollers with peripherals.
2. Assignments on programming ARM processors.
3. Design embedded systems for real – time applications.

Course Outcomes

On completion of the course, the student can

COs	Statements	K-Level
CO1	Summarize the architecture and programming of PIC microcontrollers..	K2
CO2	Explain interfacing concepts with PIC microcontrollers.	K2
CO3	Illustrate the ARM processor architecture.	K2

COs	Statements	K-Level
CO4	Build the program using the ARM Instruction Set.	K3
CO5	Develop embedded applications by interfacing peripherals.	K3

Knowledge Level: K1 – Remember, K2 – Understand, K3 – Apply, K4 – Analyze, K5 – Evaluate, K6 – Create

CO – PO Articulation Matrix

	Programme Outcomes		
	01	02	03
CO1	3	-	1
CO2	3	-	1
CO3	3	-	1
CO4	3	-	2
CO5	3	-	2
CO	3	-	1

Correlation levels 1, 2 and 3 are as defined below:

1. Slight 2. Moderate 3. Substantial (High)

Reference Books

1	Muhammad Ali Mazidi, "PIC Microcontrollers and Embedded Systems using Assembly and C for PIC18 ", Pearson Education, 2016.
2	William Hohl, "ARM Assembly Language", CRC Press, Second Edition, 2015.
3	John B. Peatman, "Design with PIC Microcontrollers", Pearson Education, Singapore –1998.
4	Andrew Sloss, Dominic Symes, and Chris Wright, "ARM System Developer's Guide Designing and Optimizing System", The Morgan Kaufmann Series, 2004.
5	Steve Furber,"ARM System-on-Chip Architecture", Addison- Wesley Professional; II Edition 2000.

P24VE2102	EMBEDDED SYSTEM DESIGN	L	T	P	C
		3	0	0	3

Course Objectives:	To understand the design challenges in embedded systems and to program the Application Specific Instruction Set Processors. To understand the bus structures and protocols, model processes using a state-machine model, and design a real-time embedded system.

Unit - I	**EMBEDDED SYSTEM OVERVIEW**	**9**

Embedded System Overview, Design Challenges – Optimizing Design Metrics, Design Methodology, RT-Level Combinational and Sequential Components, Optimizing Custom Components, Optimizing Custom Single-Purpose Processors.

Unit - II	**GENERAL AND SINGLE PURPOSE PROCESSOR**	**9**

Basic Architecture, Pipelining, Superscalar and VLIW Architectures, Programmer's View, Development Environment, Application-Specific Instruction – Set Processors (ASIPS) Microcontrollers, Timers, Counters and Watchdog Timer, UART, LCD Controllers and Analog-to- Digital Converters, Memory Concepts.

Unit - III	**BUS STRUCTURES**	**9**

Basic Protocol Concepts, Microprocessor Interfacing – I/O Addressing, Port and Bus - based I/O, Arbitration, Serial Protocols, I2C, CAN and USB, Parallel Protocols – PCI and ARM bus, Wireless Protocols – IRDA, Bluetooth, IEEE 802.11.

Unit – IV	**STATE MACHINE AND CONCURRENT PROCESS MODELS**	**9**

Basic State Machine Model, Finite-State Machine with Data path Model, Capturing State Machine in Sequential Programming Language, Program-State Machine Model, Concurrent Process Model, Communication among Processes, Synchronization among processes, RTOS – System design using RTOS.

Unit - V	**SYSTEM DESIGN**	**9**

Burglar alarm System-Design goals -Development strategy-Software development-Relevance to more complex designs- Need for emulation -Digital echo unit-Creating echo and reverb-Design requirements-Designing the codecs - The overall system design.

Total Periods:	**45**

Suggested Activities

1. Do microcontroller-based design experiments.
2. Create program –state models for different embedded applications.
3. Design and develop embedded solutions for real world problems.

Course Outcomes

On completion of the course, the student can

COs	Statements	K-Level
CO1	Summarize the knowledge of different protocols.	K2
CO2	Explain the building blocks and interfacing units of a processor.	K2
CO3	Apply networking principles in embedded devices.	K3
CO4	Make use of state machine techniques in system design using RTOS.	K3

COs	Statements	K-Level
CO5	Develop suitable embedded systems for real world applications.	K3

Knowledge Level: K1 – Remember, K2 – Understand, K3 – Apply, K4 – Analyze, K5 – Evaluate, K6 – Create

CO – PO Articulation Matrix

	Programme Outcomes		
	01	02	03
CO1	1	-	1
CO2	2	-	2
CO3	3	-	3
CO4	3	-	3
CO5	3	-	3
CO	2	-	2

Correlation levels 1, 2 and 3 are as defined below:

1. Slight 2. Moderate 3. Substantial (High)

Reference Books

1	Frank Vahid and Tony Gwargie, "Embedded System Design", John Wiley & Sons, 2009.
2	Steve Heath, "Embedded System Design", Elsevier, Second Edition, 2004.
3	Bruce Powel Douglas, "Real Time UML, Second Edition: Developing Efficient Objects for Embedded Systems", 3rd Edition 2004, Pearson Education.
4	Daniel W.Lewis, "Fundamentals of Embedded Software where C and Assembly Meet", Pearson Education, 2004.
5	Bruce Powel Douglas, "Real Time UML; Second Edition: Developing Efficient Objects for Embedded Systems", 3rd Edition 1999, Pearson Education.

P24VE2103	DIGITAL CMOS VLSI DESIGN	L	T	P	C
		3	0	2	4

Course Objectives:	To introduce the transistor-level design of all digital building blocks common to CMOS microprocessors, network processors, and the digital backend of wireless systems. To introduce the principles and design methodology in terms of the dominant circuit choices, constraints, and performance measures, while learning all important issues related to size, speed, and power consumption. Additionally, to understand the design issues of digital logic design and familiarize programming on FPGAs.

Unit - I	**MOS TRANSISTOR PRINCIPLES AND CMOS INVERTER**	**12**

MOSFET characteristic under static and dynamic conditions, MOSFET secondary effects, elmore constant, CMOS inverter-static characteristic, dynamic characteristic, power, energy, and energy delay parameters, stick diagram and layout diagrams.

Unit - II	**COMBINATIONAL LOGIC CIRCUITS**	**9**

Static CMOS design, different styles of logic circuits, logical effort of complex gates, static and dynamic properties of complex gates, interconnect delay, dynamic logic gates.

Unit - III	**SEQUENTIAL LOGIC CIRCUITS**	**9**

Static latches and registers, dynamic latches and registers, timing issues, pipelines, clocking strategies, nonbistable sequential circuits.

Unit – IV	**ARITHMETIC BUILDING BLOCKS**	**9**

Data path circuits, architectures for adders, accumulators, multipliers, barrel shifters, speed, power and area tradeoffs.

Unit - V	**MEMORY ARCHITECTURES**	**6**

Memory architectures and Memory control circuits: Read-Only Memories, ROM cells, Read-Write Memories (RAM), dynamic memory design, 6 Transistor SRAM cell, sense amplifiers-NORA CMOS Logic-TSPCL Logic.

	Total Periods:	**45**

Exp. No	Title
	Module Design using FPGA Implementation (Verilog/VHDL)
1	Adders and Subtractors
2	Multiplier (8-bit)
3	ALU circuit
4	Flip-flops
5	Universal Shift Registers
6	Asynchronous and synchronous Counters
7	Finite State Machine (Moore/Mealy) and its applications
8	Memories

Course Outcomes

On completion of the course, the student can

COs	Statements	K - Level
CO1	Explain mathematical methods and circuit analysis models in the analysis of CMOS digital circuits.	K2
CO2	Build combinational and sequential logic at the transistor level.	K3
CO3	Illustrate the design methodology of arithmetic building blocks and Memory.	K2
CO4	Construct digital circuits using CMOS logic and implement in FPGAs.	K3
CO5	Model Finite State Machine in digital circuits.	K3

Knowledge Level: K1 – Remember, K2 – Understand, K3 – Apply, K4 – Analyze, K5 – Evaluate, K6 – Create

CO – PO Articulation Matrix

	Programme Outcomes		
	01	02	03
CO1	1	-	1
CO2	1	-	2
CO3	1	-	1
CO4	3	-	3
CO5	3	-	3
CO	2	-	2

Correlation levels 1, 2 and 3 are as defined below:

1. Slight 2. Moderate 3. Substantial (High)

Reference Books

1	N.Weste, K. Eshraghian, " Principles of CMOS VLSI Design", Addison Wesley, 2nd Edition, 1993.
2	M J Smith, "Application Specific Integrated Circuits", Addison Wesley, 1997.
3	Sung-Mo Kang & Yusuf Leblebici, "CMOS Digital Integrated Circuits Analysis And Design", Mcgraw-Hill, 1998.
4	Jan Rabaey, Anantha Chandrakasan, B Nikolic, "Digital Integrated Circuits: A Design Perspective", Prentice Hall Of India, 2nd Edition, Feb 2003

P24VE2104	FPGA SYSTEM DESIGN	L	T	P	C
		3	0	2	4

Course Objectives:	Students can understand the concepts of FPGA and the need for FPGA in embedded systems. The course is designed to provide a thorough understanding and hands-on practice with FPGA-based digital system design and emulation. It aims to teach students FPGA fundamentals, including the design and implementation of circuits in them, and to understand the role of FPGAs and ASICs in embedded systems..

Unit - I	**FPGA ARCHITECTURE AND OVERVIEW**	**9**

Embedded System Design Flow - Robot Control System - Digital Design Platforms - Microprocessor Based Design - Single-Chip Computer/Microcontroller-Based Design - Application Specific Standard Products (ASSPs) - Design Using FPGA - Robotic Rover Application - FPGA Devices - FPGA and CPLD – Architecture of a Spartan-3 ETM FPGA - Floor Plan and Routing - Timing Model for a FPGA - FPGA Power Usage.

Unit - II	**EMBEDDED SYSTEM DESIGN**	**9**

FPGA-Based Embedded Processor - Design Re-Use Using On-Chip Bus Interface - Creating a Customized Microcontroller - Robot Axis Position Control - FPGA-Based Signal Interfacing and Conditioning – Motor Control Using FPGA- Case Studies for Motor Control -Prototype using FPGA- FPGA Design Test Methodology.

Unit - III	**VERILOG CONSTRUCTS**	**9**

VLSI Design Flow- Behavioral Style, the Dataflow Style, And Structural Style - Data Types - Constants - Assignment Statement - Operators - Conditional Expressions – Statement Types - Vector Operations – Bit Selects - Functions - Gate Level Modeling.

Unit – IV	**VERILOG MODELING COMBINATIONAL AND SEQUENTIAL CIRCUITS**	**9**

Combinational Logic -Adders - Multiplexers - Decoders -Comparator - ALU - UART Model, Modelling Latches and Flip Flops- Memory - Registers-Counters Modeling FSM Design Synchronous and Asynchronous - Shift Register- Test Bench Verification.

Unit - V	**FUNDAMENTALS OF SYSTEM VERILOG**	**9**

Fundamentals of SystemVerilog for Verification of RTL, Constraint Random Verification Methodology-Creating Generator, Driver, Monitor, Scoreboard, Environment Classes, Interprocess Communication and Randomization, Fundamentals of OOP's for FPGA Engineer, Layered Testbench architecture-Array, Queue, Dynamic array, Task, and Methods.

	Total Periods:	**45**

Exp. No	Title
	Module Design using FPGA Implementation (Verilog/VHDL)
1	Design Entry Using VHDL or Verilog Using HDL Languages of i. Combinational Circuits Namely 8:1 Mux/Demux, Full Adder, 8-Bit Magnitude Comparator, Encoder/Decoder, Priority Encoder. ii. Sequential Circuits Namely D-FF, 4-Bit Shift Registers (SISO, SIPO, PISO, Bidirectional), 3-Bit Synchronous Counters.
2	Test Vector Generation and Timing Analysis of Sequential and Combinational Logic Design for exercise (1) above.
3	Synthesis, P&R And Post P&R Simulation of the Components Simulated In (1) Above.
4	FPGA Implementation of PCI Bus & Arbiter. .

Exp. No	Title
5	Verifying Design Functionality Using Either Chipscope Feature (Xilinx) /the Signal Tap Feature (Altera)/Other Equivalent Feature. Invoke the PLL And Demonstrate the Use of the PLL Module for Clock Generation in FPGAs.

Course Outcomes

On completion of the course, the student can

COs	Statements	K - Level
CO1	Explain the concepts of FPGA	K2
CO2	Develop embedded system with appropriate FPGA based on real time applications	K3
CO3	Outline the fundamentals of SystemVerilog	K2
CO4	Build a combinational and sequential circuit using Verilog	K3
CO5	Make use of FPGA EDA tools for design and do the analysis of Digital Circuits	K3

Knowledge Level: K1 – Remember, K2 – Understand, K3 – Apply, K4 – Analyze, K5 – Evaluate, K6 – Create

CO – PO Articulation Matrix

	Programme Outcomes		
	01	02	03
CO1	1	-	1
CO2	3	-	3
CO3	1	-	1
CO4	2	1	3
CO5	3	1	3
CO	3	1	2

Correlation levels 1, 2 and 3 are as defined below:

1. Slight 2. Moderate 3. Substantial (High)

Reference Books

1	Rahul Dubey, "Introduction to Embedded System Design Using Field Programmable Gate Arrays" Springer-Verlag London Limited, 2009.
2	John F. Wakerly, Digital Design Principles And Practices", Pearson Education, Asia, Iii Edition, 2003.
3	Blaine Readler, "Verilog By Example: a Concise Introduction for FPGA Design", Full ARC Press,2011.
4	J. Bhasker, "A Verilog HDL Primer, Third Edition Hardcover", Star Galaxy Publishing; 3rd Edition, 2005.
5	J.Bhasker, "Verilog HDL Synthesis, a Practical Primer", Star Galaxy Publishing; 3rd Edition,1998.

P24VE2105	EMBEDDED SYSTEMS LABORATORY	L	T	P	C
		0	0	4	2
Course Objectives:	To interface sensors and display devices with a microcontroller and to program timers and UART in a microcontroller. To understand I2C and CAN protocols, concepts of scheduling, semaphores, and deadlocks using RTOS, and to design a real-time data acquisition system.				

Exp. No	Title
1	Interfacing sensors and actuators with microcontroller.
2	Configuration and programming timers and UART in microcontroller.
3	Interfacing LCD and OLED display modules with microcontroller.
4	Simulation of I2C and CAN protocols.
5	Simple task scheduling using freeware RTOS
6	Exploration on semaphores, deadlocks using RTOS.
7	Exploration of any one SOC architecture using RTOS.
8	Study of Edge AI platform on any one of the embedded processors.
9	Design of a real – time data acquisition system and control using a microcontroller.
10	Design of an IoT based system.

Course Outcomes

On completion of the course, the student can

COs	Statements	K - Level
CO1	Make use of input – output devices to interface with microcontroller.	K3
CO2	Experiment with I2C and CAN protocols.	K3
CO3	Demonstrate various concepts of RTOS.	K2
CO4	Develop a real – time data acquisition system.	K3
CO5	Construct an IoT based system.	K3

Knowledge Level: K1 – Remember, K2 – Understand, K3 – Apply, K4 – Analyze, K5 – Evaluate, K6 – Create

CO – PO Articulation Matrix

	Programme Outcomes		
	01	02	03
CO1	2	1	2
CO2	2	1	2
CO3	1	1	1

	Programme Outcomes		
	01	02	03
CO4	3	1	3
CO5	3	1	3
CO	2	1	2

Correlation levels 1, 2 and 3 are as defined below:

1. Slight 2. Moderate 3. Substantial (High)

Reference Books

1	Frank Vahid and Tony Gwargie, "Embedded System Design", John Wiley & Sons, 2009.
2	Steve Heath, "Embedded System Design", Elsevier, Second Edition, 2004.
3	Bruce Powel Douglas, "Real Time UML, Second Edition: Developing Efficient Objects for Embedded Systems", 3rd Edition 2004, Pearson Education.
4	Daniel W.Lewis, "Fundamentals of Embedded Software where C and Assembly Meet", Pearson Education, 2004.
5	Bruce Powel Douglas, "Real Time UML; Second Edition: Developing Efficient Objects for Embedded Systems", 3rd Edition 1999, Pearson Education.

P24VE2201	DESIGN FOR VERIFICATION USING UVM	L	T	P	C
		3	0	0	3
Course Objectives:	To understand the design challenges in embedded systems and to program the Application Specific Instruction Set Processors. To understand the bus structures and protocols, model processes using a state-machine model, and design a real-time embedded system.				
Unit - I	**INTRODUCTION**				**9**
Overview- The Typical UVM Testbench Architecture- The UVM Class Library-Transaction-Level Modeling (TLM) - Overview- TLM, TLM-1, and TLM-2.0 -TLM-1 Implementation- TLM-2.0 Implementation.					
Unit - II	**DEVELOPING REUSABLE VERIFICATION COMPONENTS**				**9**
Modeling Data Items for Generation - Transaction-Level Components - Creating the Driver - Creating the Sequencer - Connecting the Driver and Sequencer -Creating the Monitor - Instantiating Components- Creating the Agent - Creating the Environment -Enabling Scenario Creation -Managing of Test-Implementing Checks and Coverage.					
Unit - III	**UVM USING VERIFICATION COMPONENTS**				**9**
Creating a Top-Level Environment- Instantiating Verification Components - Creating Test Classes - Verification Component Configuration - Creating and Selecting a User-Defined Test - Creating Meaningful Tests- Virtual Sequences- Checking for DUT Correctness- Scoreboards- Implementing a Coverage Model.					
Unit – IV	**UVM USING THE REGISTER LAYER CLASSES**				**9**
Using The Register Layer Classes - Back-Door Access -Special Registers -Integrating a Register- Model in a Verification Environment- Integrating a Register Model- Randomizing Field Values- Pre- Defined Sequences.					
Unit - V	**ASSIGNMENT IN TESTBENCHES**				**9**
Assignment, APB: Protocol, Test bench Architecture, Driver and Sequencer, Monitor, Agent and Env; Creating Sequences, Building Test, Design and Testing of Top Module.					
	Total Periods:				**45**

Course Outcomes

On completion of the course, the student can

COs	Statements	K-Level
CO1	Illustrate the proficiency in designing and implementing advanced verification methodologies for embedded systems	K2
CO2	Build actual verification components for UVM	K3
CO3	Model the register layer classes for UVM.	K3
CO4	Develop testbenches using UVM.	K3
CO5	Explain the advanced peripheral bus testbenches.	K2

Knowledge Level: K1 – Remember, K2 – Understand, K3 – Apply, K4 – Analyze, K5 – Evaluate, K6 – Create

CO – PO Articulation Matrix

	Programme Outcomes		
	01	**02**	**03**
CO1	2	-	1
CO2	3	-	2
CO3	3	-	2
CO4	3	-	2
CO5	2	-	1
CO	**3**	**-**	**2**

Correlation levels 1, 2 and 3 are as defined below:

1. Slight 2. Moderate 3. Substantial (High)

Reference Books

1	The UVM Primer, An Introduction to the Universal Verification Methodology, Ray Salemi,2013.
2	SystemVerilog for Verification: A Guide to Learning the Testbench Language Features, Chris Spear, Greg Tumbush, 3rd edition, 2012.
3	https://www.udemy.com/learn-ovm-UVM/ 2.
4	http://www.testbench.in/ut_00_index.html 3.p
5	http://www.testbench.in/ot_00_index.html
6	https://www.accellera.org/images/downloads/standards/UVM/UVM_users_guide_1.2.pdf

P24VE2202	EMBEDDED AUTOMATION	L	T	P	C
		3	0	0	3

Course Objectives:	To delve into real-time embedded system design and develop proficiency in embedded C programming for 8-bit microcontrollers, while also exploring interfacing methods with peripheral devices, Furthermore, to familiarize with microcontroller programming tools and firmware, culminating in the creation of a functional home automation system.

Unit - I	**INTRODUCTION TO EMBEDDED C PROGRAMMING**	**9**

C Overview and Program Structure - C Types, Operators and Expressions - C Control Flow - C Functions and Program Structures - C Pointers and Arrays - FIFO and LIFO - C Structures - Development Tools

Unit - II	**AVR MICROCONTROLLER**	**9**

ATMEGA 16 Architecture – Non-volatile and Data Memories - Port System - Peripheral Features: Time Base, Timing Subsystem, Pulse Width Modulation, USART, SPI, Two Wire Serial Interface, ADC, Interrupts - Physical and Operating Parameters

Unit - III	**HARDWARE AND SOFTWARE INTERFACING WITH 8-BIT SERIES CONTROLLERS**	**9**

Lights and Switches - Stack Operation - Implementing Combinational Logic - Expanding I/O - Interfacing Analog to Digital Convertors - Interfacing Digital to Analog Convertors - LED Displays: Seven Segment Displays, Dot Matrix Displays - LCD Displays - Driving Relays - Stepper Motor Interface - Serial EEPROM - Real Time Clock - Accessing Constants Table - Arbitrary Waveform Generation - Communication Links - System Development Tools

Unit – IV	**VISION SYSTEM**	**9**

Fundamentals of Image Processing - Filtering - Morphological Operations - Feature Detection and Matching - Blurring and Sharpening - Segmentation - Thresholding - Contours - Advanced Contour Properties - Gradient - Canny Edge Detector - Object Detection - Background Subtraction

Unit - V	**HOME AUTOMATION**	**9**

Home Automation - Requirements - Water Level Notifier - Electric Guard Dog - Tweeting Bird Feeder - Package Delivery Detector - Web Enabled Light Switch - Curtain Automation - Android Door Lock - Voice Controlled Home Automation - Smart Lighting - Smart Mailbox - Electricity Usage Monitor -Proximity Garage Door Opener - Vision Based Authentic Entry System

	Total Periods:	**45**

Course Outcomes

On completion of the course, the student can

COs	Statements	K-Level
CO1	Interpret embedded system application using embedded C programs	K2
CO2	Explain the 8-bit series microcontroller architecture, features and pin details	K2
CO3	Illustrate hardware and software interfacing	K2
CO4	Develop the systems based on vision mechanism	K3
CO5	Build a real time home automation system	K3

Knowledge Level: K1 – Remember, K2 – Understand, K3 – Apply, K4 – Analyze, K5 – Evaluate, K6 – Create

CO – PO Articulation Matrix

	Programme Outcomes		
	01	02	03
CO1	2	-	1
CO2	2	-	1
CO3	2	-	1
CO4	3	1	2
CO5	3	1	2
CO	2	1	1

Correlation levels 1, 2 and 3 are as defined below:

1. Slight 2. Moderate 3. Substantial (High)

Reference Books

1	Dhananjay V. Gadre, "Programming and Customizing the AVR Microcontroller", McGraw-Hill, 2001.
2	Joe Pardue, "C Programming for Microcontrollers ", Smiley Micros, 2005.
3	Steven F. Barrett, Daniel J. Pack, "ATMEL AVR Microcontroller Primer: Programming and Interfacing", Morgan & Claypool Publishers, 2012.
4	Mike Riley, "Programming Your Home - Automate With Arduino, Android and Your Computer", the Pragmatic Programmers, Llc, 2012.
5	Richard Szeliski, "Computer Vision: Algorithms and Applications", Springer, 2011.
6	Kevin P. Murphy, "Machine Learning - a Probabilistic Perspective", the MIT Press Cambridge, Massachusetts, London, 2012.

P24VE2203	VLSI STRUCTURES FOR DSP	L	T	P	C
		3	0	0	3

Course Objectives:	To comprehensively understand DSP fundamentals, explore diverse DSP structures, and apply this knowledge to address the design constraints of various filters. Students will then design and optimize VLSI architectures for basic DSP algorithms, ultimately enabling them to engineer high-speed, low-power VLSI systems.

Unit - I	**INTRODUCTION TO DIGITAL SIGNAL PROCESSING**	**9**

Linear System Theory- Convolution- Correlation - DFT- FFT- Basic Concepts in FIR Filters and IIR Filters- Filter Realizations. Representation of DSP Algorithms-Block Diagram-SFG-DFG.

Unit - II	**ITERATION BOUND, PIPELINING AND PARALLEL PROCESSING OF FIR FILTER**	**9**

Data-Flow Graph Representations- Loop Bound and Iteration Bound Algorithms for Computing Iteration Bound-LPM Algorithm. Pipelining and Parallel Processing: Pipelining of FIR Digital Filters Parallel Processing - Pipelining and Parallel Processing for Low Power.

Unit - III	**RETIMING, UNFOLDING AND FOLDING**	**9**

Retiming: Definitions Properties and Problems- Solving Systems of Inequalities. Properties of Unfolding, Critical Path, Unfolding and Retiming Applications of Unfolding, Folding Transformation- Register Minimization Techniques, Register Minimization in Folded Architecture- Folding of Multi-rate System.

Unit – IV	**FAST CONVOLUTION**	**9**

Cook-Toom Algorithm- Modified Cook-Toom Algorithm. Design of Fast Convolution Algorithm by Inspection

Unit - V	**ARITHMETIC STRENGTH REDUCTION IN FILTERS**	**9**

Parallel FIR Filters-Fast FIR Algorithms-Two Parallel and Three Parallel. Parallel Architectures for Rank Order Filters -Odd Even Merge Sort Architecture-Rank Order Filter Architecture-Parallel Rank Order Filters-Running Order, Merge Order, Sorter, Low Power Rank Order Filter.

Total Periods:	**45**

Course Outcomes

On completion of the course, the student can

COs	Statements	K-Level
CO1	Explain the fundamentals of DSP processors.	K2
CO2	Summarize the overall performance of a DSP system through various transformation and optimization techniques.	K2
CO3	Explain the different types of instructions for DSP.	K2
CO4	Develop the optimized design for computation complexity and speed.	K3
CO5	Build asynchronous and wave pipelined systems considering the clock-based issues in synchronous systems	K3

Knowledge Level: K1 – Remember, K2 – Understand, K3 – Apply, K4 – Analyze, K5 – Evaluate, K6 – Create

CO – PO Articulation Matrix

	Programme Outcomes		
	01	**02**	**03**
CO1	1	-	1
CO2	1	-	1
CO3	1	-	1
CO4	3	-	2
CO5	3	-	2
CO	**2**	**-**	**1**

Correlation levels 1, 2 and 3 are as defined below:

1. Slight 2. Moderate 3. Substantial (High)

Reference Books

1	K.K Parhi: "VLSI Digital Signal Processing", John-Wiley, 2nd Edition Reprint, 2008.
2	John G.Proakis, Dimitris G.Manolakis, "Digital Signal Processing", Prentice Hall of India,1st Edition, 2009.

P24VE2204	INTERNET OF THINGS SYSTEM DESIGN	L	T	P	C
		3	0	0	3

Course Objectives:	To make students delve into IoT fundamentals and protocols, gaining theoretical and practical expertise in platform and system design. They'll explore IoT's global vision, applications, and market perspectives, utilizing gateways, devices, and data management, while also mastering state-of-the-art architecture and addressing real-world design constraints.

Unit - I	**IoT NETWORKING CORE**	**9**
Technologies Involved in IoT Development, Internet Web and Networking Technologies, Infrastructure, Overview of IoT Supported Hardware Platforms Such As: Raspberry Pi, ARM Cortex Processors, Arduino and Intel Galileo Boards, Wireless Networking Equipment and Configurations, Accessing Hardware and Device File Interactions		
Unit - II	**M2M To IoT**	**9**
Role of M2M In IoT, M2M Value Chains, IoT Value Chains, An Emerging Industrial Structure for IoT, the International Driven Global Value Chain and Global Information Monopolies. Building Architecture, Main Design Principles and Needed Capabilities, An IoT Architecture Outline, Standards Considerations.		
Unit - III	**IoT ARCHITECTURE -STATE OF THE ART**	**9**
IoT Reference Model and Architecture- Functional View, Information View, Deployment and Operational View, Other Relevant Architectural Views, Middleware Introduction-Fiware etc., Remote Monitoring and Sensing, Remote Controlling and Performance Analysis, Layering Concepts, Communication Pattern, 6LoWPAN, Sensors And Sensor Node And Interfacing Using any Embedded Target Boards (Raspberry Pi / Intel Galileo/ARM Cortex/ Arduino.		
Unit – IV	**IoT APPLICATION DEVELOPMENT**	**9**
Application Protocols: MQTT, Rest/Http, COAP, MYSQL, Back-End Application Designing Apache for Handling Http Requests, MONGODB Object Type Database, HTML, CSS & JQUERY for UI Designing, JSON Lib for Data Processing, Security & Privacy During Development		
Unit - V	**IoT SECURITY AND CASE STUDIES**	**9**
Security, Privacy and Trust in IoT-Data-Platforms for Smart Cities, First Steps Towards a Secure Platform, Smartie Approach. Data Aggregation for the IoT in Smart Cities.		
	Total Periods:	**45**

Course Outcomes

On completion of the course, the student can

COs	Statements	K-Level
CO1	Illustrate the basic structure underlying in IoT	K2
CO2	Explain the challenges in Internet of Things (IoT) system design	K2
CO3	Outline distributed embedded system hardware.	K2
CO4	Summarize the modeling approaches for real-time and IoT systems	K2
CO5	Develop the security aspects of IoT in smart applications	K3

Knowledge Level: K1 – Remember, K2 – Understand, K3 – Apply, K4 – Analyze, K5 – Evaluate, K6 – Create

CO – PO Articulation Matrix

	Programme Outcomes		
	01	02	03
CO1	1	-	1
CO2	1	-	1
CO3	2	-	1
CO4	2	-	1
CO5	3	-	2
CO	2	-	1

Correlation levels 1, 2 and 3 are as defined below:

1. Slight 2. Moderate 3. Substantial (High)

Reference Books

1	Vijay Madisetti and Arshdeepbahga, "Internet of Things (a Hands-On-Approach)", 1st Edition, Vpt, 2015.
2	Adrian Mcewen, Hakim Cassimally, "Designing the Internet of Things", November 2013, John Wiley And Sons.

P24VE2205	ANALOG IC DESIGN	L	T	P	C
		3	0	2	4

Course Objectives:	To make the students to explore CMOS analog IC fundamentals, including MOS transistor design principles, circuit choices, and trade-offs. Also to make the students to understand the topics include single and multistage amplifier design, addressing output, impedance, bandwidth, feedback, stability, and related constraints.

Unit - I	**SINGLE STAGE AMPLIFIERS**	**9**

Basic MOS physics and equivalent circuits and models, CS, CG and Source Follower, differential amplifier with active load, Cascode and Folded Cascode configurations with active load, design of Differential and Cascode Amplifiers – to meet specified SR, noise, gain, BW, ICMR and power dissipation, voltage swing, high gain amplifier structures.

Unit - II	**HIGH FREQUENCY AND NOISE CHARACTERISTICS OF AMPLIFIERS**	**9**

Miller effect, association of poles with nodes, frequency response of CS, CG and Source Follower, Cascode and Differential Amplifier stages, statistical characteristics of noise, noise in Single Stage amplifiers, noise in Differential Amplifiers.

Unit - III	**FEEDBACK AND SINGLE STAGE OPERATIONAL AMPLIFIERS**	**9**

Properties and types of negative feedback circuits, effect of loading in feedback networks, operational amplifier performance parameters, single stage Op Amps, two-stage Op Amps, input range limitations, gain boosting, slew rate, power supply rejection, noise in Op Amps.

Unit – IV	**STABILITY AND FREQUENCY COMPENSATION OF TWO STAGE AMPLIFIER**	**9**

Analysis Of Two Stage Op Amp – Two Stage Op Amp Single Stage CMOS CS as Second Stage and Using Cascode Second Stage, Multiple Systems, Phase Margin, Frequency Compensation, And Compensation of Two Stage Op Amps, Slewing in Two Stage Op Amps, Other Compensation Techniques.

Unit - V	**BANDGAP REFERENCES**	**9**

Current sinks and sources, current mirrors, Wilson current source, Widlar current source, cascode current source, design of high swing cascode sink, current amplifiers, supply independent biasing, temperature independent references, PTAT and CTAT current generation, constant-gm biasing.

	Total Periods:	**45**

Exp. No	**Title**
	Module Design using FPGA Implementation (Verilog/VHDL)
1	Design of Common Source Amplifier
2	Design of Cascade and Cascode amplifiers
3	Design of current Mirrors
4	Design of differential pair amplifier with active load
5	Design of telescopic amplifier circuit
6	Design of two-stage amplifier circuit

Course Outcomes

On completion of the course, the student can

COs	Statements	K - Level
CO1	Compare the performance of various amplifiers	K2
CO2	Explain the single stage and two stage op amps	K2
CO3	Outline current mirrors and current sinks with MOS devices	K2
CO4	Construct analog Circuit using CMOS logic with EDA tools	K3
CO5	Develop time domain and frequency domain simulations of simple analog building blocks	K3

Knowledge Level: K1 – Remember, K2 – Understand, K3 – Apply, K4 – Analyze, K5 – Evaluate, K6 – Create

CO – PO Articulation Matrix

	Programme Outcomes		
	01	02	03
CO1	1	-	1
CO2	1	-	2
CO3	1	-	1
CO4	3	1	3
CO5	3	1	3
CO	2	1	2

Correlation levels 1, 2 and 3 are as defined below:

1. Slight 2. Moderate 3. Substantial (High)

Reference Books

1	Behzad Razavi, "Design of Analog Cmos Integrated Circuits", Tata Mcgraw Hill, 2001.
2	Willey M.C. Sansen, "Analog Design Essentials", Springer, 2006.
3	Grebene, "Bipolar and MOS Analog Integrated Circuit Design", John Wiley & Sons, Inc.,2003.
4	Phillip E.Allen, Douglas R .Holberg, "CMOS Analog Circuit Design", Oxford University Press, 2nd Edition, 2002.
5	Recorded Lecture Available at http://www.ee.iitm.ac.in/vlsi/courses/ee5320_2021/start
6	Jacob Baker "CMOS: Circuit Design, Layout and Simulation, Wiley IEEE Press, 3rd Edition, 2010.

P24VE2206	EMBEDDED AUTOMATION LABORATORY	L	T	P	C
		0	0	4	2
Course Objectives:	To make the students to understand the design and development of various automation systems, enhance embedded C programming skills, and study the interfacing mechanisms of peripheral devices with microcontrollers. Also to improve the programming skills related to computer vision and to build a home automation system.				

Exp. No	Title
1	Water level controller
2	Unauthorized entry identifier
3	Tweeting bird feeder
4	Package delivery detector
5	Web enabled light switch
6	Curtain automation
7	Android door lock
8	Voice controlled home automation
9	Smart lighting
10	Smart mailbox
11	Proximity garage door opener
12	Wi Fi Managed Vehicle Parking and Theft Control

Course Outcomes

On completion of the course, the student can

COs	Statements	K - Level
CO1	Develop real time systems using microcontrollers	K3
CO2	Build the systems based on vision mechanism	K3
CO3	Construct the large and complex systems	K3
CO4	Develop a real time home automation system	K3
CO5	Demonstrate the different embedded tools	K2

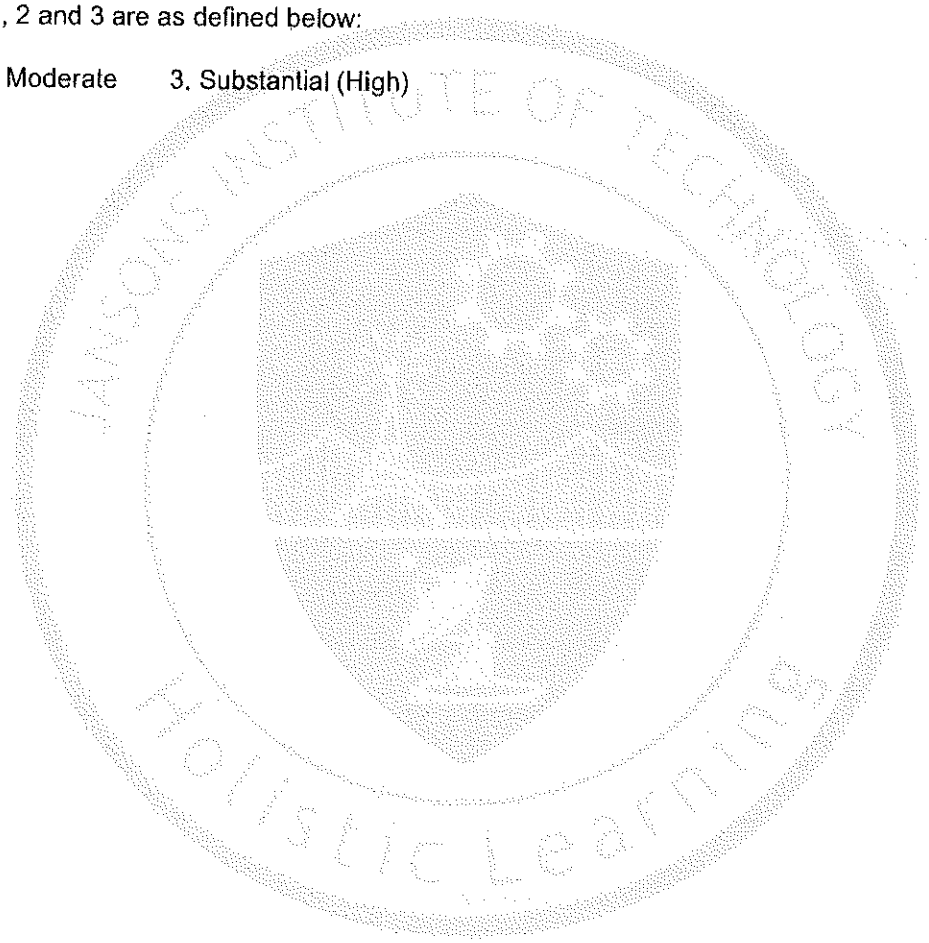
Knowledge Level: K1 – Remember, K2 – Understand, K3 – Apply, K4 – Analyze, K5 – Evaluate, K6 – Create

CO – PO Articulation Matrix

	Programme Outcomes		
	01	**02**	**03**
CO1	2	1	2
CO2	2	1	2
CO3	2	1	2
CO4	3	1	3
CO5	1	-	1
CO	**2**	**1**	**2**

Correlation levels 1, 2 and 3 are as defined below:

1. Slight 2. Moderate 3. Substantial (High)



P24VE3201	REAL TIME OPERATING SYSTEM	L	T	P	C
		3	0	2	4

Course Objectives:	To learn about the significance and usage of Real Time Operating Systems (RTOS), including different scheduling strategies and optimization principles. To understand the resource allocation or sharing processes involved in RTOS and to study the various firmware and tools related to RTOS development. Additionally, to design and develop an innovative real-time embedded system.

Unit - I	**REAL TIME EMBEDDED SYSTEMS**	**9**

Introduction - History of Real Time Systems and Embedded Systems - Real Time Services and Standards - System Resources - Analysis - Service Utility - Scheduling Classes - Cyclic Executive - Scheduler Concepts- Real Time Operating System - Thread Safe Re-entrant Functions

Unit - II	**RESOURCES AND SERVICES**	**9**

Processing - Resources - Memory –Multiresource Services: Blocking, Deadlock, Livelock, Critical Sections to Protect Shared Resources, Priority Inversion, Power Management and Processor Clock Modulation - Soft Real Time Services: Missed Deadlines, Quality of Service, Alternatives to Rate Monotonic Policy, Mixed Hard and Soft Real Time Services

Unit - III	**REAL TIME EMBEDDED COMPONENTS**	**9**

Hardware Components - Firmware Components - RTOS System Software - Software Application Components - Traditional Hard Real Time Operating Systems: Asymmetric Multicore Processing and Symmetric Multi-Core Processing - Processor Core Affinity - SMP Support Models - RTOS Hypervisors - Open-Source Real Time Operating Systems

Unit – IV	**INTEGRATING EMBEDDED LINUX**	**9**

Integrating Embedded Linux into Real Time Systems - Debugging Components - Performance Tuning - High Availability and Reliability Design - Hierarchical Approaches for Fail-Safe Design.

Unit - V	**CASE STUDIES**	**9**

System Life Cycle - Continuous Media Applications - Video and Audio Processing – Robotic Applications - Computer Vision Applications

	Total Periods:	**45**

Exp. No	Title
1	Implement a Linux process that is executed at the default priority for a user-level application and waits on a binary semaphore to be given by another application. Run this process and verify its state using the ps command to list its process descriptor. Now, run a separate process to give the semaphore causing the first process to continue execution and exit. Verify completion.
2	Create An Application That Creates Two Tasks That Wait On a Timer Whilst the Main Task Loops.
3	Develop an Applications Using Linux
4	Design of Plant Control System

Course Outcomes

On completion of the course, the student can

COs	Statements	K - Level
CO1	Summarize of scheduling algorithm and process	K2
CO2	Explain on firmware and tools related to the development of RTOS	K2
CO3	Develop an embedded system with RTOS functionality	K3
CO4	Construct systems in Linux environments	K3
CO5	Build large real-time embedded systems	K3

Knowledge Level: K1 – Remember, K2 – Understand, K3 – Apply, K4 – Analyze, K5 – Evaluate, K6 – Create

CO – PO Articulation Matrix

	Programme Outcomes		
	01	02	03
CO1	2	-	1
CO2	1	-	1
CO3	3	-	2
CO4	3	1	2
CO5	3	1	3
CO	2	1	2

Correlation levels 1, 2 and 3 are as defined below:

1. Slight 2. Moderate 3. Substantial (High)

Reference Books

1	Sam Siewert, John Pratt, "Real-Time Embedded Components and Systems with Linux and Rtos", Mercury Learning and Information Llc, 2016.
2	Jonathan W. Valvano, "Embedded Systems: Real Time Operating Systems for ARM Cortex-M Microcontrollers", Createspace Independent Publishing Platform, Fourth Edition, 2017.
3	Giorgio C. Buttazzo, "Hard Real-Time Computing Systems - Predictable Scheduling Algorithms and Applications", Springer Science+Buisness Media, LLC, Third Edition, 2011.
4	Albert M. K. Cheng, "Real-Time Systems - Scheduling, Analysis and Verification", a John Wiley & Sons Inc Publication, 2002.
5	Wang K.C., "Embedded and Real Time Operating System", Springer, 2017

P24VE3202	EMBEDDED NETWORKING	L	T	P	C
		3	0	2	4

Course Objectives:	To learn the concepts of serial and parallel communication protocols and to understand application development using USB and CAN bus for PIC microcontrollers. To learn the basics of Ethernet and application development using embedded internet, as well as wireless sensor network communication protocols.

Unit - I	COMMUNICATION PROTOCOLS	9

Serial/Parallel Communication – Serial Communication Protocols -RS 232 Standard – RS 485 – Synchronous Serial Protocols -Serial Peripheral Interface (SPI) – Inter Integrated Circuits (I2C) – PC Parallel Port Programming - PCI Bus Protocol.

Unit - II	USB AND CAN BUS	9

USB Bus – Introduction – Speed Identification On the Bus – USB States – USB Bus Communication: Packets –Data Flow Types –Enumeration –Descriptors –PIC Microcontroller USB Interface – CAN Bus – Introduction - Basic Concepts & Definitions-Identifiers & Arbitration- Robustness & Flexibility-Message Formats-Error Handling -PIC Microcontroller CAN Interface –a Simple Application with CAN.

Unit - III	ETHERNET BASICS	9

Elements of a Network – Inside Ethernet – Building a Network: Hardware Options – Cables, Connections and Network Speed – Design Choices: Selecting Components –Ethernet Controllers – Using the Internet In Local And Internet Communications – Inside the Internet Protocol.

Unit – IV	EMBEDDED ETHERNET	9

Exchanging Messages Using UDP And TCP – Serving Web Pages With Dynamic Data – Serving Web Pages That Respond To User Input – Email for Embedded Systems – Using FTP.

Unit - V	EMBEDDED WIRELESS SENSOR NETWORKS	9

Wireless Sensor Networks –Introduction To WSN-Challenges for WSNs - Characteristic Requirements – Required Mechanisms - Single-Node Architecture -Hardware Components-Energy Consumption of Sensor Nodes-Operating Systems and Execution Environments-Some Examples of Sensor Nodes.

	Total Periods:	45

Exp. No	Title
	Module Design using FPGA Implementation (Verilog/VHDL)
1	Write a Simple Application Program USB and PIC Interface.
2	Write a Simple Application Program Using CAN And PCI.
3	Write a Program for Email Transferring Using UDP And TCP
4	Write a Program for Energy Harvesting In WSN Node
5	Develop An Application Using Embedded Wireless Sensor Networks

Course Outcomes

On completion of the course, the student can

COs	Statements	K - Level
CO1	Compare wired and wireless network protocols	K2
CO2	Summarize the embedded networking concepts with USB and CAN bus	K2
CO3	Explain the Embedded Wireless Sensor networks	K2
CO4	Demonstrate the communication between two networks	K3
CO5	Build an wireless sensor network	K3

Knowledge Level: K1 – Remember, K2 – Understand, K3 – Apply, K4 – Analyze, K5 – Evaluate, K6 – Create

CO – PO Articulation Matrix

	Programme Outcomes		
	01	02	03
CO1	1	-	1
CO2	2	-	1
CO3	2	-	1
CO4	3	1	3
CO5	3	1	3
CO	2	1	2

Correlation levels 1, 2 and 3 are as defined below:

1. Slight 2. Moderate 3. Substantial (High)

Reference Books

1	Jan Axelson, "Embedded Ethernet and Internet Complete", Penram Publications, 2003.
2	Bhaskar Krishnamachari, Networking, Wireless Sensors - Cambridge Press 2005.
3	Olaf Pfeiffer, Andrew Ayre and Christian Keydel, "Embedded Networking With CAN And CAN Open", Second Edition Published By Copperhill Media Corporation, 2003.
4	Holgerkarl, Andreas Willig, "Protocols and Architectures for Wireless Sensor Networks", John Wiley,2005.
5	Frank Vahid, Tony Givargis, "Embedded Systems Design: a Unified Hardware/Software Introduction" - John & Wiley Publications, 2006
6	Jan Axelson, "Parallel Port Complete: Programming, Interfacing and Using the PCs Parallel Printer Port" - Penram Publications, 1996.
7	Dogan Ibrahim, "Advanced PIC Microcontroller Projects In C: From USB To RTOS With the PIC18f Series" - Elsevier 2008.

P24VE3203	DEEP LEARNING	L	T	P	C
		3	0	2	4

Course Objectives:	Develop and train deep neural networks, including CNN, R-CNN, Fast R-CNN, Faster R-CNN, and Mask R-CNN for detection and recognition. Build and train RNNs, work with NLP and word embeddings, and understand the internal structure of LSTM and GRU and their differences. Additionally, explore autoencoders for image processing.

Unit - I	DEEP LEARNING CONCEPTS	6

Fundamentals about Deep Learning. Perception Learning Algorithms. Probabilistic modelling. Early Neural Networks. How Deep Learning different from Machine Learning. Scalars. Vectors. Matrixes, Higher Dimensional Tensors. Manipulating Tensors. Vector Data. Time Series Data. Image Data. Video Data.

Unit - II	NEURAL NETWORKS	9

About Neural Network. Building Blocks of Neural Network. Optimizers. Activation Functions. Loss Functions. Data Pre-processing for neural networks, Feature Engineering. Overfitting and Underfitting. Hyperparameters.

Unit - III	CONVOLUTIONAL NEURAL NETWORK	10

About CNN. Linear Time Invariant. Image Processing Filtering. Building a convolutional neural network. Input Layers, Convolution Layers. Pooling Layers. Dense Layers. Backpropagation Through the Convolutional Layer. Filters and Feature Maps. Backpropagation Through the Pooling Layers. Dropout Layers and Regularization. Batch Normalization. Various Activation Functions. Various Optimizers. LeNet, AlexNet, VGG16, ResNet. Transfer Learning with Image Data. Transfer Learning using Inception Oxford VGG Model, Google Inception Model, Microsoft ResNet Model. RCNN, Fast R-CNN, Faster R-CNN, Mask-RCNN, YOLO.

Unit – IV	NATURAL LANGUAGE PROCESSING USING RNN	10

About NLP & its Toolkits. Language Modeling. Vector Space Model (VSM). Continuous Bag of Words (CBOW). Skip-Gram Model for Word Embedding. Part of Speech (PoS) Global Cooccurrence Statistics–based Word Vectors. Transfer Learning. Word2Vec. Global Vectors for Word Representation GloVe. Backpropagation Through Time. Bidirectional RNNs (BRNN) . Long Short Term Memory (LSTM). Bi-directional LSTM. Sequence-to-Sequence Models (Seq2Seq). Gated recurrent unit GRU.

Unit - V	DEEP REINFORCEMENT & UNSUPERVISED LEARNING	10

About Deep Reinforcement Learning. Q-Learning. Deep Q-Network (DQN). Policy Gradient Methods. Actor-Critic Algorithm. About Autoencoding. Convolutional Auto Encoding. Variational Auto Encoding. Generative Adversarial Networks. Autoencoders for Feature Extraction. Auto Encoders for Classification. Denoising Autoencoders. Sparse Autoencoders.

	Total Periods:	45

Exp. No	Title
1	Feature Selection from Video and Image Data
2	Image and video recognition
3	Image Colorization
4	Aspect Oriented Topic Detection & Sentiment Analysis
5	Object Detection using Autoencoder

Course Outcomes

On completion of the course, the student can

COs	Statements	K - Level
CO1	Illustrate the concepts of deep learning.	K2
CO2	Explain about neural network basics and its construction.	K2
CO3	Infer reinforcement and unsupervised learning.	K3
CO4	Build real time system using image processing concepts.	K3
CO5	Demonstrate aspect Oriented Topic Detection and Sentiment Analysis.	K3

Knowledge Level: K1 – Remember, K2 – Understand, K3 – Apply, K4 – Analyze, K5 – Evaluate, K6 – Create

CO – PO Articulation Matrix

	Programme Outcomes		
	01	02	03
CO1	2	-	1
CO2	2	-	1
CO3	2	-	1
CO4	3	1	2
CO5	3	1	2
CO	2	1	1

Correlation levels 1, 2 and 3 are as defined below:

1. Slight 2. Moderate 3. Substantial (High)

Reference Books

1	Deep Learning A Practitioner's Approach Josh Patterson and Adam Gibson O'Reilly Media, Inc.2017.
2	Learn Keras for Deep Neural Networks, Jojo Moolayil, Apress,2018.
3	Deep Learning Projects Using TensorFlow 2, Vinita Silaparasetty, Apress, 2020.
4	Deep Learning with Python, FRANÇOIS CHOLLET, MANNING SHELTER ISLAND,2017.
5	Pro Deep Learning with TensorFlow, Santanu Pattanayak, Apress,2017.

P24VE3204	REAL TIME EMBEDDED SYSTEMS	L	T	P	C
		3	0	2	4

Course Objectives:	To understand the basics of embedded systems and ARM architecture, including RTOS concepts like scheduling and memory management. To learn about the programming aspects of RTOS and different protocols of embedded wireless applications. Additionally, to grasp concepts involved in the design of hardware and software components for an embedded system..

Unit - I	INTRODUCTION	9

Real Time System – Embedded Systems – Architecture of Embedded System – Simple Programming for Embedded System – Process of Embedded System Development – Pervasive Computing – Information Access Devices – Smart Cards – Microcontrollers – ARM Processor -Real Time Microcontrollers.

Unit - II	EMBEDDED/REAL TIME OPERATING SYSTEM	9

Operating System Concepts: Processes, Threads, Interrupts, Events - Real Time Scheduling Algorithms - Memory Management – Overview of Operating Systems for Embedded, Real Time Handheld Devices – Target Image Creation – Programming In Linux, Rtlinux, Vxworks, Microcontroller Operating System Overview.

Unit - III	CONNECTIVITY	9

Wireless Connectivity - Bluetooth – Other Short-Range Protocols – Wireless Application Environment – Service Discovery – Middleware.

Unit – IV	REAL TIME UML	9

The Rapid Object-Oriented Process for Embedded Systems (ROPES) Process. MDA and Platform-Independent Models- Scheduling Model-Based Projects- Model Organization Principles- Working with Model-Based Projects - Object Orientation with UML 2.0-Structural Aspects-Object Orientation with UML 2.0-Dynamic Aspects-UML Profile for Schedulability, Performance, and Time. Requirements Analysis – Object Identification Strategies – Object Behaviour – Real Time Design Patterns.

Unit - V	SOFTWARE DEVELOPMENT AND APPLICATION	9

Concurrency – Exceptions – Tools – Debugging Techniques – Optimization –Interfacing Digital Camera with USB Port. Interfacing of Sensors and Actuators for a Real Time Industrial Application.

	Total Periods:	45

Exp. No	Title
1	Read Input from Switch and Automatic Control/Flash LED for ARM Processor
2	Laboratory Exercises on Task Scheduling
3	Simple Program in Linux, Rtlinux and Vxworks
4	Develop a Real Time Security Monitoring System

Course Outcomes

On completion of the course, the student can

COs	Statements	K - Level
CO1	Infer the choice of suitable embedded processor for a given application	K2
CO2	Build the hardware and software for the embedded system	K3

COs	Statements	K - Level
CO3	Develop the real time kernel/operating system functions, task control block structure and study the different task states	K3
CO4	Construct different types of inter task communication and synchronization techniques	K3
CO5	Demonstrate the aspects of embedded connectivity in real time systems	K3

Knowledge Level: K1 – Remember, K2 – Understand, K3 – Apply, K4 – Analyze, K5 – Evaluate, K6 – Create

CO – PO Articulation Matrix

	Programme Outcomes		
	01	02	03
CO1	1	-	1
CO2	2	-	2
CO3	3	-	2
CO4	3	1	3
CO5	3	1	3
CO	**2**	**1**	**2**

Correlation levels 1, 2 and 3 are as defined below:

1. Slight 2. Moderate 3. Substantial (High)

Reference Books

1	R.J.a.Buhr, D.L.Bailey, "An Introduction to Real-Time Systems", Prentice-Hall International,1999.
2	David E-Simon, "An Embedded Software Primer", Pearson Education, 2007.
3	C.M.Krishna, Kang G.Shin, "Real Time Systems", Mc-Graw Hill, 2010.
4	B.P.Douglass, "Real Time UML - Advances In the UML for Real-Time Systems, 3rd Edition Addison-Wesley, 2004.
5	K.V.K. Prasad, "Embedded/Real Time Systems: Concepts, Design and Programming", Dream Tech Press, Black Book, 2005.
6	R.Barnett, L.O.Cull, S.Cox, "Embedded C Programming and the Microchip PIC", Thomason Learning, 2004.
7	Wayne Wolf, "Computers as Components - Principles of Embedded Computer System Design", Mergen Kaufmann Publisher, 2006.
8	Sriram V Iyer, Pankaj Gupta, "Embedded Real Time Systems Programming", Tata Mc-Graw Hill, 2004.

P24VE3205	PERVASIVE COMPUTING	L	T	P	C
		3	0	2	4

Course Objectives:	To understand the characteristics and principles of pervasive computing and the solutions currently in use. To recognize the role of wireless protocols in shaping the future internet and to design and implement pervasive applications. Additionally, to introduce the enabling technologies of pervasive computing.

Unit - I	PERVASIVE COMPUTING CONCEPTS	9

Perspectives of Pervasive Computing, Challenges, Technology; the Structure and Elements of Pervasive Computing Systems: Infrastructure and Devices, Middleware for Pervasive Computing Systems, Pervasive Computing Environments.

Unit - II	CONTEXT COLLECTION, USER TRACKING, AND CONTEXT REASONING	9

Resource Management in Pervasive Computing: Efficient Resource Allocation In Pervasive Environments, Transparent Task Migration, Implementation and Illustrations.

Unit - III	HCI INTERFACE IN PERVASIVE ENVIORNMENTS	9

HCI Service and Interaction Migration, Context- Driven HCI Service Selection, Scenario Study: Video Calls at a Smart Office, a Web Service– Based HCI Migration Framework.

Unit – IV	PERVASIVE MOBILE TRANSACTIONS	9

Mobile Transaction Framework, Context-Aware Pervasive Transaction Model, Dynamic Transaction Management, Formal Transaction Verification, Evaluations

Unit - V	CASE STUDIES	9

ICAMPUS Prototype, IPSPACE: AN IPV6-Enabled Intelligent Space

	Total Periods:	45

Exp. No	Title
1	To design the Software for Mobile Phones Using Symbion OS i.Text String Handling ii.Graphical Application iii.Dialog Application iv.Drawing Application v.File Handling Operations
2	Application Level- To Study New HCI Techniques for Small Mobile Devices and Embedded Devices
3	Case Studies- Projects in Pervasive Computing- to explore wearable and handheld computing and their enabling technologies

Course Outcomes

On completion of the course, the student can

COs	Statements	K - Level
CO1	Outline the basic problems, performance requirements of pervasive computing applications and	K2

COs	Statements	K - Level
	the trends of pervasive computing and its impacts on future computing applications and society.	
CO2	Compare the performance of different data dissemination techniques and algorithms for mobile real-time applications	K2
CO3	Explain about concepts of IPSPACE, IPV6	K2
CO4	Develop Symbion OS based software application for mobile phone to perform basic activities	K3
CO5	Build a real time wearable and handheld computing device	K3

Knowledge Level: K1 – Remember, K2 – Understand, K3 – Apply, K4 – Analyze, K5 – Evaluate, K6 – Create

CO – PO Articulation Matrix

	Programme Outcomes		
	01	02	03
CO1	1	-	1
CO2	1	-	1
CO3	2	-	1
CO4	3	1	3
CO5	3	1	3
CO	2	1	2

Correlation levels 1, 2 and 3 are as defined below:

1. Slight 2. Moderate 3. Substantial (High)

Reference Books

1	Minyi Guo, Jingyu Zhou, Feilong Tang, Yao Shen ,"Pervasive Computing: Concepts, Technologies and Applications", CRC Press, 2016.
2	Obaidat, Mohammad S., Mieso Denko, And Isaac Woungang, Eds. Pervasive Computing and Networking. John Wiley & Sons, 2011.
3	Laurence T. Yang, Handbook On Mobile and Ubiquitous Computing Status and Perspective, 2012, CRC Press.
4	Seng Loke, Context-Aware Computing Pervasive Systems, Auerbach Pub., New York, 2007.
5	Uwe Hansmann Etl , Pervasive Computing, Springer, New York, 2001.

P24VE3206	PHYSICAL DESIGN AUTOMATION	L	T	P	C
		3	0	2	4

Course Objectives:	To understand the concepts of physical design processes such as partitioning, floor planning, placement, and routing. Discuss the concepts of design optimization algorithms and their application to physical design automation. Understand the concepts of simulation and synthesis in VLSI design automation, and formulate CAD design problems using algorithmic methods.

Unit - I	**INTRODUCTION**	**9**

Layout and Design Rules, Materials for VLSI Fabrication, Basic Algorithmic Concepts for Physical Design, Physical Design Processes and Complexities. Partition: Kernigham-Lin's Algorithm, Fiduccia Mattheyes Algorithm, Krishnamurthy Extension, Hmetis Algorithm, Multilevel Partition Techniques.

Unit - II	**FLOOR-PLANNING**	**9**

Planning: Hierarchical Design, Wire Length Estimation, Slicing and Non-Slicing Floor Plan, Polar Graph Representation, Operator Concept, Stockmeyer Algorithm for Floor Planning, Mixed Integer Linear Program.

Unit - III	**PLACEMENT**	**9**

Design Types: ASICS, SOC, Microprocessor RLM; Placement Techniques: Simulated Annealing, Partition Based, Analytical, and Hall's Quadratic; Timing and Congestion Considerations

Unit – IV	**ROUTING**	**9**

Detailed, Global and Specialized Routing, Channel Ordering, Channel Routing Problems and Constraint Graphs, Routing Algorithms, Yoshimura and Kuh's Method, Zone Scanning and Net Merging, Boundary Terminal Problem, Minimum Density Spanning Forest Problem, Topological Routing, Cluster Graph Representation.

Unit - V	**SEQUENTIAL LOGIC OPTIMIZATION AND CELL BINDING**	**9**

State Based Optimization, State Minimization, Algorithms; Library Binding and Its Algorithms, Concurrent Binding.

	Total Periods:	**45**

Exp. No	Title
1	**Graph Algorithms** Graph Search Algorithms Spanning Tree Algorithm Shortest Path Algorithm Steiner Tree Algorithm
2	**Partitioning Algorithms** Group Migration Algorithms Simulated Annealing and Evolution Algorithms Metric Allocation Method
3	**Floor Planning Algorithms** Constraint Based Methods Integer Programming Based Method Rectangular Dualization Based Methods Hierarchical Tree Based Methods Simulated Evolution Algorithms Time Driven Floor Planning Algorithms
4	**Routing Algorithms**

Exp. No	Title
	Two Terminal Algorithms Multi Terminal Algorithm

Course Outcomes

On completion of the course, the student can

COs	Statements	K - Level
CO1	Explain about the placing and partitioning of blocks while designing the layout for IC.	K2
CO2	Identify the performance issues in circuit layout.	K3
CO3	Develop automation algorithms for partitioning, floor planning, placement and routing based on physical design problems	K3
CO4	Construct the decomposer for large mapping problem into pieces, including logic optimization with partitioning, placement and routing	K3
CO5	Build circuits using both analytical and CAD tools	K3

Knowledge Level: K1 – Remember, K2 – Understand, K3 – Apply, K4 – Analyze, K5 – Evaluate, K6 – Create

CO – PO Articulation Matrix

	Programme Outcomes		
	01	02	03
CO1	2	-	1
CO2	2	-	1
CO3	3	-	2
CO4	3	1	2
CO5	3	1	2
CO	3	1	2

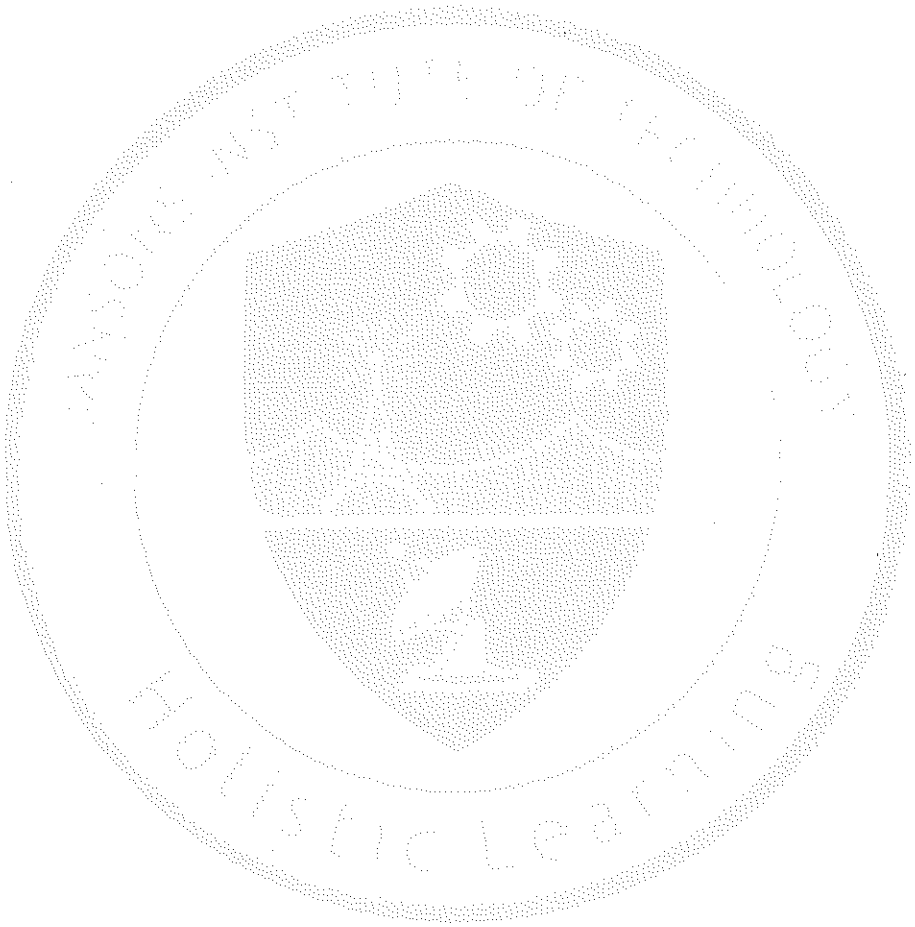
Correlation levels 1, 2 and 3 are as defined below:

1. Slight 2. Moderate 3. Substantial (High)

Reference Books

1	Sarrafzadeh, M. and Wong, C.K, "An Introduction to VLSI Physical Design", 4th Edition, Mc Graw-Hill
2	Wolf. W, "Modern VLSI Design System on Silicon", 2nd Ed., Pearson Education.

3	Dreschler, "Evolutionary Algorithms for VLSI CAD", 3rd Edition, Springer.
4	Sait, S.M, And Youssef, "VLSI Physical Design Automation: Theory and Practice", 1999, World Scientific Publishing Company.
5	Sherwani, "Algorithms for VLSI Physical Design Automation", 2nd Edition, Kluwer



P24AC7001	ENGLISH FOR RESEARCH PAPER WRITING	L	T	P	C
		2	0	0	0

Course Objectives:	Teach how to improve writing skills and level of readability and to impart the writing skills. Infer the skills needed when writing the Conclusion and ensure the quality of paper at very first-time submission.

Unit - I	**INTRODUCTION TO RESEARCH PAPER WRITING**	**6**
Planning and Preparation, Word Order, breaking up long sentences, Structuring Paragraphs and Sentences, Being Concise and Removing Redundancy, Avoiding Ambiguity and Vagueness		
Unit - II	**PRESENTATION SKILLS**	**6**
Clarifying Who Did What, Highlighting Your Findings, Hedging and Criticizing, Paraphrasing and Plagiarism, Sections of a Paper, Abstracts, Introduction		
Unit - III	**TITLE WRITING SKILLS**	**6**
Key skills are needed when writing a Title, key skills are needed when writing an Abstract, key skills are needed when writing an Introduction, skills needed when writing a Review of the Literature, Methods, Results, Discussion, Conclusions, The Final Check		
Unit – IV	**RESULT WRITING SKILLS**	**6**
Skills are needed when writing the Methods, skills needed when writing the Results, skills are needed when writing the Discussion, skills are needed when writing the Conclusions		
Unit - V	**VERIFICATION SKILLS**	**6**
Useful phrases, checking Plagiarism, how to ensure paper is as good as it could possibly be the first- time submission		
	Total Periods:	**30**

Course Outcomes

On completion of the course, the student can

COs	Statements	K-Level
CO1	Interpret writing meaningful sentences and coherent paragraphs.	K2
CO2	Outline the paraphrasing and plagiarism for presentation skills.	K2
CO3	Summarize about review literature, write methodology, results and conclusion.	K2
CO4	Illustrate how to write methodology, discussions, results and conclusion.	K2
CO5	Infer how to use useful phrases and checking plagiarism	K2

Knowledge Level: K1 – Remember, K2 – Understand, K3 – Apply, K4 – Analyze, K5 – Evaluate, K6 – Create

CO – PO Articulation Matrix

	Programme Outcomes		
	01	02	03
CO1	2	1	3

	Programme Outcomes		
	01	02	03
CO2	2	2	3
CO3	3	2	2
CO4	2	1	3
CO5	3	2	2
CO	2	2	3

Correlation levels 1, 2 and 3 are as defined below:

1. Slight 2. Moderate 3. Substantial (High)

Reference Books

1	Adrian Wallwork, English for Writing Research Papers, Springer New York Dordrecht Heidelberg London, 2011
2	Day R How to Write and Publish a Scientific Paper, Cambridge University Press 2006
3	Goldbort R Writing for Science, Yale University Press (available on Google Books) 2006
4	Highman N, Handbook of Writing for the Mathematical Sciences, SIAM. Highman's book 1998.

P24AC7002	DISASTER MANAGEMENT	L	T	P	C
		2	0	0	0

Course Objectives:	To explain the critical understanding of key concepts in disaster risk reduction and humanitarian response and to illustrate disaster risk reduction and humanitarian response policy and practice from multiple perspectives. To understand standards of humanitarian response and practical relevance in specific types of disasters and conflict situations.

Unit - I	**INTRODUCTION**	**6**
Disaster: Definition, Factors and Significance; Difference between Hazard and Disaster; Natural and Manmade Disasters: Difference, Nature, Types and Magnitude.		
Unit - II	**REPERCUSSIONS OF DISASTERS AND HAZARDS**	**6**
Economic Damage, Loss of Human and Animal Life, Destruction of Ecosystem. Natural Disasters: Earthquakes, Volcanisms, Cyclones, Tsunamis, Floods, Droughts and Famines, Landslides and Avalanches, Man-made disaster: Nuclear Reactor Meltdown, Industrial Accidents, Oil Slicks and Spills, Outbreaks of Disease and Epidemics, War and Conflicts.		
Unit - III	**DISASTER PRONE AREAS IN INDIA**	**6**
Study of Seismic Zones; Areas Prone to Floods and Droughts, Landslides and Avalanches; Areas Prone to Cyclonic and Coastal Hazards with Special Reference to Tsunami; Post-Disaster Diseases and Epidemics.		
Unit – IV	**DISASTER PREPAREDNESS AND MANAGEMENT**	**6**
Preparedness: Monitoring of Phenomena Triggering a Disaster or Hazard; Evaluation of Risk: Application of Remote Sensing, Data from Meteorological and Other Agencies, Media Reports: Governmental and Community Preparedness.		
Unit - V	**RISK ASSESSMENT**	**6**
Disaster Risk: Concept and Elements, Disaster Risk Reduction, Global and National Disaster Risk Situation. Techniques of Risk Assessment, Global Co-Operation in Risk Assessment and Warning, People's Participation in Risk Assessment. Strategies for Survival		
	Total Periods:	**30**

Course Outcomes

On completion of the course, the student can

COs	Statements	K-Level
CO1	Summarize the basics of disaster.	K2
CO2	Explain a critical understanding of key concepts in disaster risk reduction and humanitarian response.	K2
CO3	Illustrate the disaster risk reduction and humanitarian response policy.	K2
CO4	Summarize the standards of humanitarian response and practical relevance in disaster and conflict situations.	K2
CO5	Outline the disaster risk assessment approaches.	K2

Knowledge Level: K1 – Remember, K2 – Understand, K3 – Apply, K4 – Analyze, K5 – Evaluate, K6 – Create

CO – PO Articulation Matrix

	Programme Outcomes		
	01	**02**	**03**
CO1	2	2	2
CO2	2	1	2
CO3	1	2	2
CO4	2	1	3
CO5	1	2	2
CO	**2**	**2**	**2**

Correlation levels 1, 2 and 3 are as defined below:

1. Slight 2. Moderate 3. Substantial (High)

Reference Books

1	Goel S. L., Disaster Administration and Management Text and Case Studies", Deep & Deep Publication Pvt. Ltd., New Delhi, 2009.
2	Nishitha Rai, Singh AK, "Disaster Management in India: Perspectives, issues and strategies "'New Royal book Company, 2007.
3	Sahni, Pradeep Et.Al.," Disaster Mitigation Experiences and Reflections", Prentice Hall of India, New Delhi, 2001.

P24AC7003	CONSTITUTION OF INDIA	L	T	P	C
		2	0	0	0

Course Objectives:	To understand the premises informing the twin themes of liberty and freedom from a civil rights perspective and to address the growth of Indian opinion regarding modern Indian intellectuals' constitution. To infer the role and entitlement of civil and economic rights as well as the emergence of nationhood in the early years of Indian nationalism.

Unit - I	**HISTORY OF MAKING OF THE INDIAN CONSTITUTION**	**3**
History, Drafting Committee, (Composition & Working)		
Unit - II	**PHILOSOPHY OF THE INDIAN CONSTITUTION**	**3**
Preamble, Salient Features		
Unit - III	**CONTOURS OF CONSTITUTIONAL RIGHTS AND DUTIES**	**5**
Fundamental Rights, Right to Equality, Right to Freedom, right against Exploitation, Right to Freedom of Religion, Cultural and Educational Rights, Right to Constitutional Remedies, Directive Principles of State Policy, Fundamental Duties.		
Unit – IV	**ORGANS OF GOVERNANCE**	**5**
Parliament, Composition, Qualifications and Disqualifications, Powers and Functions, Executive, President, Governor, Council of Ministers, Judiciary, Appointment and Transfer of Judges, Qualifications, Powers and Functions.		
Unit - V	**LOCAL ADMINISTRATION AND ELECTION COMMISSION**	**14**
District's Administration head: Role and Importance, Municipalities: Introduction, Mayor and role of Elected Representative, CEO, Municipal Corporation. Pachayati raj: Introduction, PRI: Zila Panchayat. Elected officials and their roles, CEO Zila Pachayat: Position and role. Block level: Organizational Hierarchy (Different departments), Village level: Role of Elected and Appointed officials, Importance of grass root democracy. Election Commission: Role and Functioning. Chief Election Commissioner and Election Commissioners - Institute and Bodies for the welfare of SC/ST/OBC and women.		
	Total Periods:	**30**

Course Outcomes

On completion of the course, the student can

COs	Statements	K-Level
CO1	Outline the history of the Indian constitution.	K2
CO2	Summarize the philosophy of the Indian constitution.	K2
CO3	Infer the concepts of fundamental rights and directive principles of state policy.	K2
CO4	Interpret the importance of organs of governance.	K2
CO5	Explain the local administration and election commission.	K2

Knowledge Level: K1 – Remember, K2 – Understand, K3 – Apply, K4 – Analyze, K5 – Evaluate, K6 – Create

CO – PO Articulation Matrix

	Programme Outcomes		
	01	**02**	**03**
CO1	1	1	2
CO2	1	1	2
CO3	2	2	3
CO4	2	1	2
CO5	1	2	2
CO	**1**	**1**	**2**

Correlation levels 1, 2 and 3 are as defined below:

1. Slight 2. Moderate 3. Substantial (High)

Reference Books

1	The Constitution of India,1950(Bare Act), Government Publication.
2	Dr.S.N.Busi, Dr.B. R.Ambedkar framing of Indian Constitution,1st Edition, 2015.
3	M.P. Jain, Indian Constitution Law, 7th Edn., LexisNexis,2014.
4	D.D. Basu, Introduction to the Constitution of India, LexisNexis, 2015.

P24AC7004	நற்றமிழ் இலக்கியம்	L	T	P	C
		2	0	0	0

Unit - I	சங்க இலக்கியம்	6

1 தமிழின் துவக்க நூல் தொல்காப்பியம்
- எழுத்து, சொல், பொருள்

2 அகநானூறு (82)
- இயற்கை இன்னிசை அரங்கம்

3 குறிஞ்சிப் பாட்டின் மலர்க்காட்சி

4 புறநானூறு (95, 195)
- போரை நிறுத்திய ஔவையார்

Unit - II	அறநெறித் தமிழ்	6

1. அறநெறி வகுத்த திருவள்ளுவர்
- அறம் வலியுறுத்தல், அன்புடைமை, ஒப்புறவு அறிதல், ஈகை, புகழ்

2. பிற அறநூல்கள் - இலக்கிய மருந்து
- ஏலாதி, சிறுபஞ்சமூலம், திரிகடுகம், ஆசாரக்கோவை (தூய்மையை வலியுறுத்தும் நூல்)

Unit - III	இரட்டை காப்பியங்கள்	6

1 கண்ணகியின் புரட்சி
- சிலப்பதிகார வழக்குரை காதை

2 சமூகசேவை இலக்கியம் மணிமேகலை
- சிறைக்கோட்டம் அறக்கோட்டமாகிய காதை

Unit – IV	அருள்நெறித் தமிழ்	6

1. சிறுபாணாற்றுப்படை
- பாரி முல்லைக்குத் தேர் கொடுத்தது, பேகன் மயிலுக்குப் போர்வை கொடுத்தது, அதியமான் ஔவைக்கு நெல்லிக்கனி கொடுத்தது, அரசர் பண்புகள்

2. நற்றிணை
- அன்னைக்குரிய புன்னை சிறப்பு

3. திருமந்திரம் (617, 618)
- இயமம் நியமம் விதிகள்

4. தர்மச்சாலையை நிறுவிய வள்ளலார்

5. புறநானூறு
- சிறுவனே வள்ளலானான்

6. அகநானூறு (4) - வண்டு
நற்றிணை (11) - நண்டு
கலித்தொகை (11) - யானை, புறா
ஐந்திணை 50 (27) - மான்
ஆகியவை பற்றிய செய்திகள்

Unit - V	நவீன தமிழ் இலக்கியம்	6

1. உரைநடைத் தமிழ்,
   - தமிழின் முதல் புதினம்,
   - தமிழின் முதல் சிறுகதை,
   - கட்டுரை இலக்கியம்,
   - பயண இலக்கியம்.
   - நாடகம்,
2. நாட்டு விடுதலை போராட்டமும் தமிழ் இலக்கியமும்,
3. சமுதாய விடுதலையும் தமிழ் இலக்கியமும்,
4. பெண் விடுதலையும் விளிம்பு நிலையினரின் மேம்பாட்டில் தமிழ் இலக்கியமும்,
5. அறிவியல் தமிழ்
6. இணையத்தில் தமிழ்,
7. சுற்றுச்சூழல் மேம்பாட்டில் தமிழ் இலக்கியம்.

Total Periods:	30

தமிழ் இலக்கிய வெளியீடுகள் / புத்தகங்கள்

1	தமிழ் இணைய கல்விக்கழகம் (Tamil Virtual University) www.tamilvu.org
2	தமிழ் விக்கிப்பீடியா (Tamil Wikipedia) -https://ta.wikipedia.org
3	தர்மபுர ஆதீன வெளியீடு
4	வாழ்வியல் களஞ்சியம் - தமிழ்ப் பல்கலைக்கழகம், தஞ்சாவூர்.
5	தமிழ்கலைக் களஞ்சியம் - தமிழ் வளர்ச்சித் துறை (thamilvalarchithurai.com)
6	அறிவியல் களஞ்சியம் - தமிழ்ப் பல்கலைக்கழகம், தஞ்சாவூர்.

Skill development.
collaboration with foreign institutions